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DATA SHEET

SAA4978H
Picture Improved Combined Network (PICNIC)

Product specification
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PHILIPS

Picture Improved Combined Network (PICNIC) SAA4978H

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Picture Improved Combined Network (PICNIC)

SAA4978H

1 FEATURES

- Clamp
- Analog AGC
- Triple YUV 9-bit Analog-to-Digital Converter (ADC)
- Triple bypassable analog anti-alias filter
- 4 MHz notch filter
- Non-linear phase filter after ADC
- 4 : 1 : 1 or 4 : 2 : 2 digital processing
- 4 : 1 : 1 or 4 : 2 : 2 selectable I/O interface
- Asynchronous digital input
- Time base correction
- Histogram analysis
- Histogram modification
- Subtitle detection
- Black bar detection
- Line memory based noise reduction (spatial)
- Noise level measurement
- Clamp noise reduction
- Dynamic peaking
- Energy measurement
- Multi Picture-In-Picture (multi PIP) decimation
- Differential Pulse Code Modulation (DPCM) data decompression for colour
- 2D-peaking and coring
- Non-linear phase filter before DAC
- Coaxial Transceiver Interface (CTI)
- Triple 10-bit Digital-to-Analog Converter (DAC)
- Triple bypassable analog reconstruction filter
- Embedded microcontroller (80C51 core)
- Programmable signal positioner
- SNERT interface
- I^2C-bus user control interface
- Boundary Scan Test (BST).

2 GENERAL DESCRIPTION

The SAA4978H is a monolithic integrated circuit suitable either for $1f_H$ or $2f_H$ applications that contain a large variety of picture improvement functions. It combines analog-to-digital and digital-to-analog conversion for YUV signals, digital processing, line-locked clock regeneration and an 80C51 microcontroller core in one IC.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDA}	analog supply current	V_{DDA} = 3.45 V	–	145	180	mA
I_{DDD}	digital supply current	V_{DDD} = 3.6 V	–	210	270	mA
f_{clk}	clock frequency		–	16	–	MHz
S/N	signal-to-noise ratio	default settings	50	–	–	dB

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4978H	QFP160	plastic quad flat package; 160 leads (lead length 1.6 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT322-2

5 BLOCK DIAGRAM

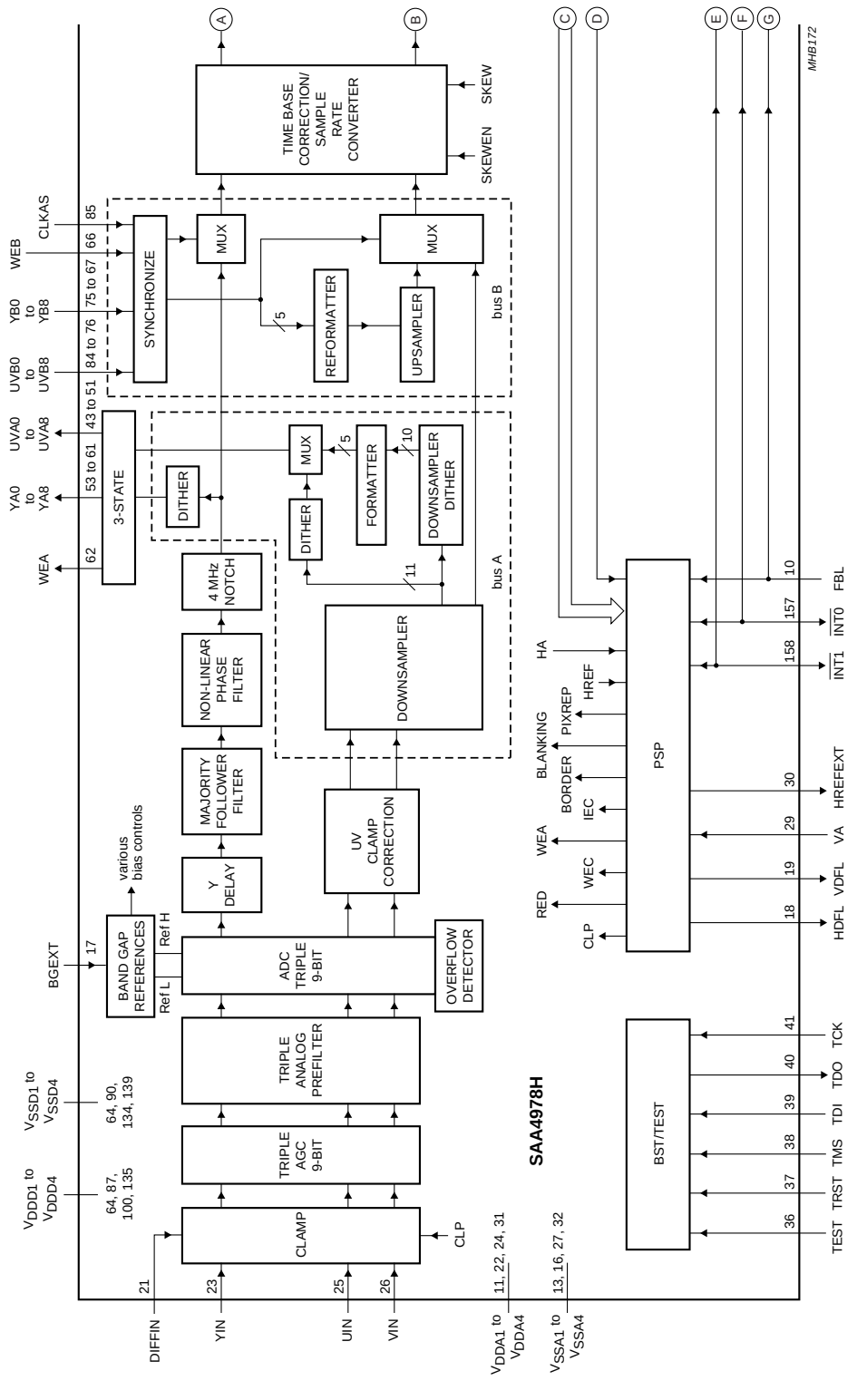


Fig.1 Block diagram (continued in Fig.2).

Standard bus width in data path is 9 bits; exceptions are marked.

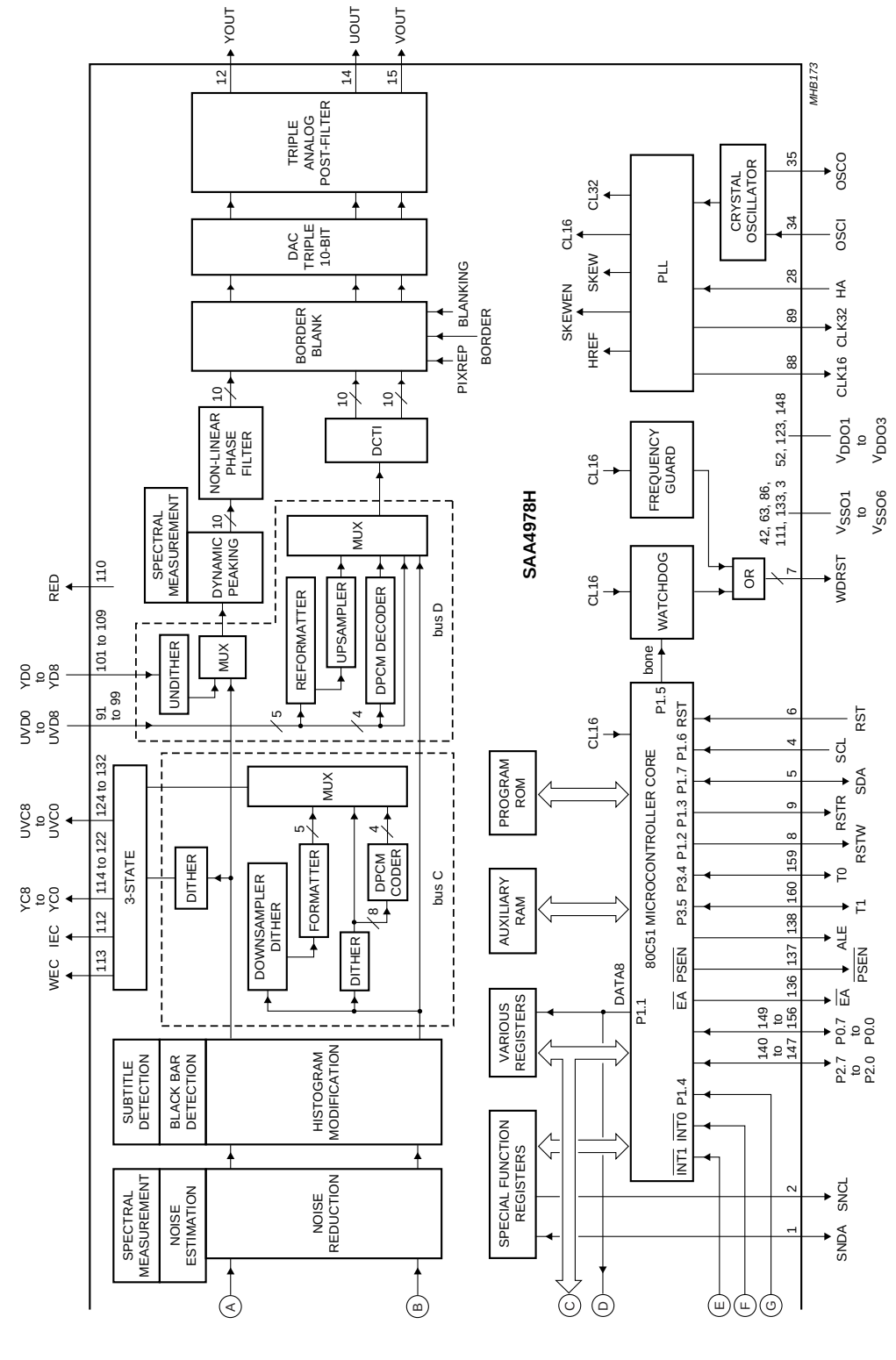


Fig.2 Block diagram (continued from Fig.1).

Standard bus width in data path is 9 bits; exceptions are marked.

6 PINNING INFORMATION

SYMBOL	PIN	DESCRIPTION
SNDA	1	SNERT data input/output
SNCL	2	SNERT clock output
V_{SSO6}	3	digital microcontroller I/O ground 6; internally connected to all other V_{SSO} pins
SCL	4	I^2C-bus serial clock input (P1.6)
SDA	5	I^2C-bus serial data input/output (P1.7)
RST	6	microcontroller reset input
WDRST	7	watchdog reset output
RSTW	8	reset write signal output/SNERT reset (only PALplus) Port 1.2
RSTR	9	reset read signal output/SNERT reset (SAA4991WP or SAA4992H) Port 1.3
FBL	10	fast blanking input to PSP and Port 1.4
V_{DDA1}	11	analog back-end supply voltage 1
YOUT	12	Y analog output
V_{SSA1}	13	analog back-end ground 1
UOUT	14	U analog output
VOUT	15	V analog output
V_{SSA2}	16	analog input ground 2; internally connected to substrate
BGEXT	17	band gap external/reference currents input
HDFL	18	horizontal synchronization signal output, deflection part
VDFL	19	vertical synchronization signal output, deflection part
AGND	20	analog ground
DIFFIN	21	differential Y input
V_{DDA2}	22	analog input supply voltage 2
YIN	23	Y analog input
V_{DDA3}	24	analog input supply voltage 3
UIN	25	U analog input
VIN	26	V analog input
V_{SSA3}	27	analog input ground 3; internally connected to substrate
HA	28	horizontal synchronization input, acquisition part
VA	29	vertical synchronization input, acquisition part
HREFEXT	30	horizontal reference external output
V_{DDA4}	31	analog PLL supply voltage 4
V_{SSA4}	32	analog PLL ground 4; internally connected to substrate
V_{SSX}	33	oscillator ground
OSCI	34	oscillator input
OSCO	35	oscillator output
TEST	36	test input/external 32 MHz clock input
TRST	37	BST reset input
TMS	38	BST test mode select input
TDI	39	BST test data input
TDO	40	BST test data output

SYMBOL	PIN	DESCRIPTION
TCK	41	BST test clock input
V_{SSO1}	42	digital bus A/B ground 1; internally connected to all other V_{SSO} pins
UVA0	43	bus A output UVL
UVA1	44	bus A output UV0
UVA2	45	bus A output UV1
UVA3	46	bus A output UV2
UVA4	47	bus A output UV3
UVA5	48	bus A output UV4
UVA6	49	bus A output UV5
UVA7	50	bus A output UV6
UVA8	51	bus A output UV7
V_{DDO1}	52	digital I/O bus A/B supply voltage 1; internally connected to all other V_{DDO} pins
YA0	53	bus A output YL
YA1	54	bus A output Y0
YA2	55	bus A output Y1
YA3	56	bus A output Y2
YA4	57	bus A output Y3
YA5	58	bus A output Y4
YA6	59	bus A output Y5
YA7	60	bus A output Y6
YA8	61	bus A output Y7
WEA	62	write enable bus A output
V_{SSO2}	63	digital bus A/B ground 2; internally connected to all other V_{SSO} pins
V_{DDD1}	64	digital core supply voltage 1; internally connected to all other V_{DDD} pins
V_{SSD1}	65	digital core ground 1; internally connected to all other V_{SSD} pins
WEB	66	write enable bus B input
YB8	67	bus B input Y7
YB7	68	bus B input Y6
YB6	69	bus B input Y5
YB5	70	bus B input Y4
YB4	71	bus B input Y3
YB3	72	bus B input Y2
YB2	73	bus B input Y1
YB1	74	bus B input Y0
YB0	75	bus B input YL
UVB8	76	bus B input UV7
UVB7	77	bus B input UV6
UVB6	78	bus B input UV5
UVB5	79	bus B input UV4
UVB4	80	bus B input UV3
UVB3	81	bus B input UV2

SYMBOL	PIN	DESCRIPTION
UVB2	82	bus B input UV1
UVB1	83	bus B input UV0
UVB0	84	bus B input UVL
CLKAS	85	asynchronous clock input
V_{SSO3}	86	digital I/O bus B/clock ground 3; internally connected to all other V_{SSO} pins
V_{DDD2}	87	digital core supply voltage 2; internally connected to all other V_{DDD} pins
CLK16	88	16 MHz clock output
CLK32	89	32 MHz clock output
V_{SSD2}	90	digital core ground 2; internally connected to all other V_{SSD} pins
UVD0	91	bus D input UVL
UVD1	92	bus D input UV0
UVD2	93	bus D input UV1
UVD3	94	bus D input UV2
UVD4	95	bus D input UV3
UVD5	96	bus D input UV4
UVD6	97	bus D input UV5
UVD7	98	bus D input UV6
UVD8	99	bus D input UV7
V_{DDD3}	100	digital core supply voltage 3; internally connected to all other V_{DDD} pins
YD0	101	bus D input YL
YD1	102	bus D input Y0
YD2	103	bus D input Y1
YD3	104	bus D input Y2
YD4	105	bus D input Y3
YD5	106	bus D input Y4
YD6	107	bus D input Y5
YD7	108	bus D input Y6
YD8	109	bus D input Y7
RED	110	read enable bus D output
V_{SSO4}	111	digital I/O bus C/D ground 4; internally connected to all other V_{SSO} pins
IEC	112	input enable bus C output
WEC	113	write enable bus C output
YC8	114	bus C output Y7
YC7	115	bus C output Y6
YC6	116	bus C output Y5
YC5	117	bus C output Y4
YC4	118	bus C output Y3
YC3	119	bus C output Y2
YC2	120	bus C output Y1
YC1	121	bus C output Y0
YC0	122	bus C output YL

SYMBOL	PIN	DESCRIPTION
V_{DDO2}	123	digital I/O supply voltage 2 to bus C/D; internally connected to all other V_{DDO} pins
UVC8	124	bus C output UV7
UVC7	125	bus C output UV6
UVC6	126	bus C output UV5
UVC5	127	bus C output UV4
UVC4	128	bus C output UV3
UVC3	129	bus C output UV2
UVC2	130	bus C output UV1
UVC1	131	bus C output UV0
UVC0	132	bus C output UVL
V_{SSO5}	133	digital I/O ground 5 to bus D and microcontroller; internally connected to all other V_{SSO} pins
V_{SSD3}	134	digital core ground 3; internally connected to all other V_{SSD} pins
V_{DDD4}	135	digital core supply voltage 4; internally connected to all other V_{DDD} pins
$\overline{EA}$	136	external access output (active LOW)
$\overline{PSEN}$	137	program store enable output (active LOW)
ALE	138	address latch enable output
V_{SSD4}	139	digital core ground 4; internally connected to all other V_{SSD} pins
P2.7	140	Port 2 data input/output signal 7
P2.6	141	Port 2 data input/output signal 6
P2.5	142	Port 2 data input/output signal 5
P2.4	143	Port 2 data input/output signal 4
P2.3	144	Port 2 data input/output signal 3
P2.2	145	Port 2 data input/output signal 2
P2.1	146	Port 2 data input/output signal 1
P2.0	147	Port 2 data input/output signal 0
V_{DDO3}	148	microcontroller I/O pad supply voltage 3
P0.7	149	Port 0 data input/output signal 7
P0.6	150	Port 0 data input/output signal 6
P0.5	151	Port 0 data input/output signal 5
P0.4	152	Port 0 data input/output signal 4
P0.3	153	Port 0 data input/output signal 3
P0.2	154	Port 0 data input/output signal 2
P0.1	155	Port 0 data input/output signal 1
P0.0	156	Port 0 data input/output signal 0
$\overline{INT0}$	157	interrupt 0, I/O Port 3.2 (active LOW)
$\overline{INT1}$	158	interrupt 1, I/O Port 3.3 (active LOW)
T0	159	timer 0 I/O Port 3.4
T1	160	timer 1 I/O Port 3.5

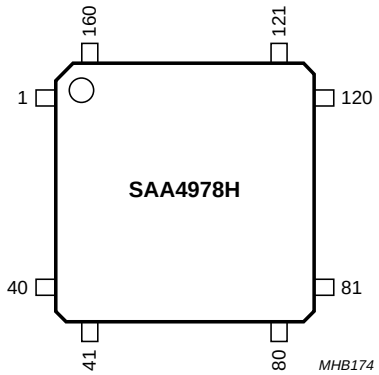


Fig.3 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The SAA4978H consists of the following main functional blocks:

- Analog preprocessing and analog-to-digital conversion
- Digital processing at $1f_H$ level
- Digital processing at $2f_H$ level
- Digital-to-analog conversion
- Line-locked clock generation
- Crystal oscillator
- Control interfacing I^2C-bus and SNERT
- Register I/O
- Programmable Signal Positioner (PSP)
- 80C51 microcontroller core
- Board level testability provisions.

7.1 Analog input blocks

7.1.1 Gain elements for automatic gain control (9 dB range)

A variable amplifier is used to map the possible YUV input range to the analog-to-digital converter range e.g. as defined for SCART signals.

According to this specification, a lift of 6 dB up to a drop of 3 dB may be necessary with respect to the nominal values. The gain setting within the required minimum 9 dB range is performed digitally via the internal microcontroller. For this purpose a gain setting digital-to-analog converter is incorporated. The smallest step in the gain setting should be hardly visible on the picture, this can be met with smaller steps of 0.4%/step.

Luminance and chrominance gain settings can be separately controlled. The reason for this split is that U and V may have already been gain adjusted by an Automatic Chrominance Control (ACC), whereas luminance is to be adjusted by the SAA4978H AGC. However, for RGB originated sources, Y, U and V should be adjusted with the same AGC gain.

7.1.2 Clamp circuit, clamping Y to digital level 32 and UV to 0 (twos complement)

A clamp circuit is applied to each input channel, to map the colourless black level in each video line (on the sync back porch) to level 32 at 9 bits for Y and to the centre level of the converters for U and V. During the clamp period, an internally generated clamp pulse is used to switch-on the clamp action.

A voltage controlled current source construction, which references to voltage reference points in the ladders of the analog-to-digital converters, provides a current on the input of the YUV signals in order to bring the signals to the correct DC value. This current is proportional to the DC error, but is limited to ±150 μA. It is essential that the clamp current becomes zero with a zero error and that the asymmetry between positive and negative clamp currents is limited to within 10%. When the clamping action is off, the residual clamp current should be very low, so that the clamp level will not drift away within a video line.
The clamp level in the Y channel has a minimum value of 600 mV to ensure undisturbed clamping for maximum Y input signals with top sync levels up to 600 mV. In order to improve common mode rejection it is recommended to connect the same source impedance as used in the YIN input at the DIFFIN input to ground.

7.1.3 Analog anti-aliasing prefilter

A 3rd-order linear phase filter is applied to each of the Y, U and V channels. It provides a notch on f_{clk} (16 MHz at Y, U and V) to strongly prevent aliasing to low frequencies, which would be the most disturbing.
The bandwidth of the filters is designed for –3 dB at 5.6 MHz. The filters can be bypassed if external filtering with other characteristics is desired. In the bypass mode the gain accuracy of the front-end part is 4% instead of 8% for the filter-on mode.

7.1.4 9-bit analog-to-digital conversion

Three identical multi-step type analog-to-digital converters are used to convert the Y, U and V inputs with a 16 MHz data rate. The ADCs have a 2-bit overflow detection, and an underflow detection for U and V, to be used for AGC control. The 2 bits are coded for one in-range level and three overflow levels; 1 dB, 1 to 2 dB and 2 to 3 dB.

7.2 Digital processing blocks

7.2.1 Overflow detection

A histogram of the three overflow levels is made every field and can be read in a 2-byte accuracy. An input selector defines which ADC is monitored.

In the event of U or V selection the underflow information is also added to the first histogram level, in this way the data can be handled as out-of-range information.

The histogram content provides information for the AGC to make an accurate estimate of the decrease in gain, in the event of overflow for luminance or out-of-range detection for U and V.

7.2.2 Y delay

The Y samples can be shifted onto 4 positions with respect to the UV samples. This shift is meant to account for a possible difference in delay prior to the SAA4978H, e.g. from a prefilter in front of an analog-to-digital converter. The zero delay setting is suitable for the nominal case of aligned input data according to the interface format standard. One setting provides one sampleless delay in Y, the other two settings provide more delay in the Y path.

7.2.3 Transient noise suppression

A circuit is added in the luminance channel to suppress the typical multi-step trip level noise. This majority follower filter compares the neighbouring pixels to a +1 or –1 LSB difference. If the majority of these differences is +1 then 1 is added to the actual pixel. If the majority of these differences is –1 then 1 is subtracted from the actual pixel. The number of pixels included in the filter is selectable; 1 (bypass), 3, 5, 7 or 9.

7.2.4 Non-linear phase filter after ADC

The non-linear phase filter adjusts for possible group delay differences in the luminance channel. The filter coefficients are $[-L \times (1 - u); 1 + L; -L \times u]$; where L determines the strength of the filter and u determines the asymmetry. The effect of the asymmetry is that for higher frequencies the delay is decreased for $u \leq 0.5$. Settings are provided for L = 0, $1/16$, $2/16$ and $3/16$ and u = 0, $1/4$ and $1/2$.

7.2.5 4 MHz notch

The 4 MHz notch provides a zero on $1/4$ of the sample frequency. With f_s = 16 MHz the notch is thus at 4 MHz. The 3 dB notch width is 2 MHz. The filter coefficients are $1/8 \times [-1; 0; 5; 0; 5; 0; -1]$. This filter gives a relative gain of 0.75 dB at 1.7 and 6.3 MHz.

The notch can be bypassed without changing the group delay.

7.2.6 Digital clamp correction for UV

During 32 samples within the active clamping the clamp error is measured and accumulated to determine a low-pass filtered value of the clamp error. A vertical recursive filter is then used to further reduce this error value. This value can be read by the microcontroller or be used directly to correct the clamp error. It is also possible for the microcontroller to give a fixed correction value.

7.2.7 4 : 4 : 4 DOWNSAMPLED TO 4 : 2 : 2 OR 4 : 1 : 1

4 : 4 : 4 data is downsampled to 4 : 2 : 2, by first filtering with a [1; 0; –7; 0; 38; 64; 38; 0; –7; 0; 1] filter, before being subsampled by a factor of 2. The U and V samples from the 4 : 2 : 2 data are filtered again by a [–1; 0; 9; 16; 9; 0; –1] filter, before being subsampled a second time by a factor of 2. Bypassing this function keeps the data in the 4 : 2 : 2 format.

7.2.8 BUS A FORMAT: INTERFACE FORMATTING, TIMED WITH ENABLING SIGNAL (see Table 1 and Fig.9)

The chosen 4 : 1 : 1 or 4 : 2 : 2 formatted output data is presented to bus A (YUV_A bus), consistent with the WEA data enable signal. After the rising edge of WEA the first, respectively second, data word contains the first phase of the 4 : 1 : 1 or 4 : 2 : 2 format, depending on the qualifier respectively prequalifier mode of WEA. If the data has to be formatted to 8 bits, a choice can be made between rounding and dithered rounding. Dithered rounding may be applied in the sense that every odd output sample has had an addition of 0.25 LSB (relative to 8 bits) before truncation and every even output sample has had an addition of 0.75 LSB before truncation. In this way, on average, correct rounding is realized (no DC shift). Especially for low frequency signals, the resolution is increased by a factor of 2 by the high frequency modulation. The phase of dithering can be switched 180° from line-to-line, field-to-field or frame-to-frame, in order to decrease the visibility of the dithering pattern.

The not connected output pins of bus A, including WEA (depending on the application), can be set to 3-state to allow short-circuiting of these pins at board production. Short-circuiting at not connected outputs can not be tested by Boundary Scan Test (BST). For outputs in 3-state mode it is not allowed to apply voltages higher than V_{DDO} + 0.3 V.

7.2.9 BUS B FORMAT (see Table 1 and Fig.9)

Bus B can accommodate the following formats; 4 : 1 : 1 serial, 4 : 2 : 2 parallel, 4 : 2 : 2 double clock UYVY, all synchronous and asynchronous. All external formats are selectable with prequalifier or qualifier WEB. All of the various input formats are converted to the internal 9 bits 4 : 2 : 2. For the 8-bit inputs, the LSB of the input bus should be connected externally to a fixed logic level. In the event of a 4 : 1 : 1 input, the U and V channels are reformatted and upsampled by generating the extra samples with a $\frac{1}{16} \times$ [–1; 9; 9; –1] filter. The other U and V samples remain equal to the original 4 : 1 : 1 sample values.

It is possible, in bus B reformatter, to invert the UV data so that the SAA4978H can handle any polarity convention of the UV data.

In the event of an asynchronous input the clock has to be provided externally to pin CLKAS.

When applying an external PALplus decoder with 30 ms processing delay, the vertical field start can be set via software in a PSP register. For *"CCIR 656"* standard data format input, inversion of the MSB of the (synchronized) bus B UV input can be selected. Synchronization signals included in this format will be ignored.

7.2.10 TIME BASE CORRECTION AND SAMPLE RATE CONVERSION

The Time Base Correction (TBC) and Sample Rate Conversion (SRC) block provides a dynamically controlled delay with an accuracy of up to $\frac{1}{64}$ of a pixel and a range of –0.5 to +0.5 lines (plus processing delay).

The time base correction block has an input for skew data. This skew data can be the phase error measured by a HPLL, which is located in the PLL block of the SAA4978H. The skew is used as a shift of the complete active video part of a line. Added with a static (user controlled) shift, up to $\frac{1}{2}$ video line (32 µs) can be shifted in both directions, related to a nominal $\frac{1}{2}$ line delay.

For sample rate conversion, the delay is also varied along the line with the subpixel accuracy. With a zero-order variation of the delay, a linear compress or expand function can be obtained. The range for the compression factor is 0 to 2, meaning infinite zoom up to a compression with a factor of 2. With a 2nd-order variation of the delay added to the control, the compression factor can be modulated with a parabolic shape, thus giving a panoramic view option to display e.g. 4 : 3 video on a 16 : 9 screen or vice versa.

The static shift may also be used to make the delay of the SAA4978H plus periphery equal to an integer number of lines. This is useful for $1f_H$ applications, in which the horizontal sync signal is not delayed with the video data. This will then make the function of time base correction obsolete for $1f_H$ applications.

Another main task for the sample rate converter is to resynchronize external data at a non-system clock sample rate, for instance, MPEG decoder signals at 13.5 MHz. A requirement for these signals is that they are line and frame locked to the SAA4978H.

7.2.11 NOISE REDUCTION

The noise reduction part consists of clamp noise reduction and spatial noise reduction for low frequency noise. Within this ensemble a two dimensional band split is used, enabling also the functions of 2D low passing, adding the multi Picture-In-Picture (multi PIP) function and 2D peaking.

The clamp noise reduction is realized with an adaptive temporal recursive filter. This filter will correct the DC level of each line when it is varying from field-to-field in the segments with the least likely movement. This clamp noise filtering is intended to correct for clamp errors in a complete chain, which cannot be removed with traditional clamping on the back porch of the video. Clamp noise is only reduced for luminance.

The spatial noise reduction is targeted for reduction of the mid frequency noise spectrum, where adaptive filtering combines pixels around the centre pixel and pixels from the lines above in a recursive way. This spatial noise reduction is only realized for luminance.

The 2D low-pass filter is a [1; 2; 1] filter in both the horizontal and vertical direction. 2D high-pass is realized by taking the centre tap and subtracting the 2D low-pass output from it. Also added in the 2D high-pass is the vertical low-passed data, which is subtracted from the centre tap and multiplied by a user selectable gain (0 to $^{7}/_{8}$). The 2D high-pass data is multiplied by a user selectable gain of 0 and $^{2}/_{4}$ to $^{8}/_{4}$ and cored before adding it to the 2D low-pass branch for the 2D peaking function. The HF signal bypasses both the LF temporal and the spatial noise reduction, therefore sharpness in the high frequencies is not reduced by the noise reduction parts. The factor 0 on the HF signal yields a pure 2D low-passed signal at the output. Multi PIP with pure subsampling of this signal yields a much better result than without the low-pass operation.

7.2.12 HISTOGRAM

Histogram modification consists of acquiring the histogram of the luminance levels and correcting the luminance transfer curve in order to provide more perceptual contrast in the picture.

For economy, a subsampling is realized on the video with a factor of 4 before the histogram is produced. From line-to-line, a two pixel offset is used on the subsample pattern.

The histogram acquisition uses 32 baskets on the grey scale from (ultra) black to (ultra) white. Pixels that are found around the centre of a basket increase a counter for that basket with the value 8, pixels that come around the edge between two baskets increase the counters in both baskets, such as 3 in the left one and 5 in the right one. By this method, the quantization distortion is overcome from having a discrete set of baskets.

Between acquisition of the histogram and correction of the transfer curves, the microcontroller included in the SAA4978H processes the counter values from the 32 baskets. The outcome of the microcontrollers algorithm defines a differential transfer curve for the luminance. This means that only differences from a 1 : 1 transfer curve are coded. This is done in 32 LUT points, with a linear interpolation for all input values in between the LUT points.

When changes are made to the luminance level of pixels, the saturation has to be restored by using the same relative gain for the U and V channels.

The histogram data also provides the information of the minimum and maximum levels of Y, U and V, by which the microcontroller can affect an AGC gain before the video analog-to-digital conversion.

Another main part of the histogram is the display-bars block. This block can insert up to 32 horizontal bars in the YUV data path. Size, spacing, luminance, colour and length are fully programmable. This can be used to construct a visual display of the histogram or transfer curve.

7.2.13 SUBTITLE DETECTION

Subtitle detection searches in a large area of the video field for patterns that are characteristic for subtitles. The expectation is to encounter in a video line a considerable number of crossings through both a dark grey and a light grey threshold and in its vicinity also crossings in the other direction. This part is realized with valid crossing (event) counting on each line in the target area. This event value is stored for 128 lines in the subtitle RAM, which is located at the top of the auxiliary RAM. The subtitle logic has higher priority to access the subtitle RAM than the microcontroller.

The internal microcontroller can filter out this data. In a number of adjacent lines, there must be a similar high count value for the number of events. If this condition holds then the detection of subtitles on that vertical position is more definite.

This information can be used in combination with other information on how to display the video source on the screen. Such decisions are made entirely by the internal microcontroller.

7.2.14 BLACK BAR DETECTION

Black bar detection searches in the upper and in the lower part of the screen to respectively the last black line and the first black line. To avoid disturbances of Logos in the video, measurements can be performed in only the horizontal centre part of the lines.

7.2.15 BUS C FORMAT (see Table 1)

The U and V samples from the 4 : 2 : 2 data are filtered again by a [–1; 0; 9; 16; 9; 0; –1] filter, before being subsampled by a factor of 2. Bypassing this function keeps the data in the 4 : 2 : 2 format.

Should it be required to format the data to 8 bits, a choice can be made between rounding and dithered rounding. Dithered rounding may be applied in the sense that every odd output sample has had an addition of 0.25 LSB (relative to 8 bits) before truncation and every even output sample has had an addition of 0.75 LSB before truncation. In this way, normally, correct rounding is realized (no DC shift). Especially for low frequency signals, the resolution is increased by a factor of 2 by the high frequency modulation. The phase of dithering is switched 180° from line-to-line, field-to-field or frame-to-frame in order to decrease the visibility of the dithering pattern.

This block also performs the subsampling for multi PIP, with subsampling factors of 1, 2, 3 and 4.

Another output format at bus C is Differential Pulse Code Modulation (DPCM) 4 : 2 : 2. This data compression method is applied on the U and V channels, and gives a 50% data reduction. In this way it is possible to convert a 4 : 2 : 2 picture to $2f_H$ using a single 12-bit wide field memory. This format is especially useful for graphics conversion with high amplitude and high saturation input signals. The not connected output pins of bus C including WEC and IEC (depending on the application) can be set to 3-state to allow short-circuiting of these pins at board production. Short-circuiting at not connected outputs can not be tested by BST. For outputs in 3-state mode it is not allowed to apply voltages higher than V_{DDO} + 0.3 V.

7.2.16 BUS D REFORMATTER: THE VARIOUS INPUT FORMATS ARE ALL CONVERTED TO THE INTERNAL 9 BITS 4 : 2 : 2 (see Table 1)

Bus D can handle 4 : 1 : 1 external 8 or 9 bits, 4 : 2 : 2 external 8 or 9 bits, 4 : 2 : 2 internal 9 bits and DPCM 4 : 2 : 2.

Bus D is selectable in $1f_H$ and $2f_H$ mode. In $1f_H$ mode the internal input can also be used.

For dithered 8-bit luminance signals an undither block is provided that restores the 9th bit for low frequency and low noise. This is needed before the peaking circuit to prevent amplification of the $\frac{1}{2}f_s$ dither modulation.

In the event of 8-bit inputs, the LSB of the input bus should be externally connected to a fixed logic level.

In the event of a 4 : 1 : 1 input, the U and V channels are reformatted and upsampled by generating the extra samples with a $\frac{1}{16} \times$ [–1; 9; 9; –1] filter. The other U and V samples remain equal to the original 4 : 1 : 1 sample values.

7.2.17 PEAKING

Peaking in the SAA4978H can be used in two ways:

1. The first way is to give the luminance a linear boost of the higher frequency ranges, which makes no distinction between small and large details or edges.
2. The second way is to use the peaking dynamically, in order to boost smaller details and provide less gain on large details and edges. The effect is detail enhancement without the creation of unnaturally large overshoots and undershoots on large details and edges.

Basically, the three peaking filters (1 high-pass and 2 band-pass) filter the incoming luminance signal. The high-pass filter is made with [–1; 2; –1] coefficients, giving a maximum throughput at $\frac{1}{2}f_s$ (equals 8 MHz). The first band-pass filter has [–1; 0; 2; 0; –1] coefficients, giving a maximum throughput at $\frac{1}{4}f_s$ (equals 4 MHz). The second band-pass filter has a cascade of [–1; 0; 0; 2; 0; 0; –1] and [1; 2; 1] coefficients, giving a maximum throughput at 2.38 MHz.

With a separate gain control on each of the peaking filters [possible gain settings of (0, $\frac{1}{16}$, $\frac{2}{16}$, $\frac{3}{16}$, $\frac{4}{16}$, $\frac{5}{16}$, $\frac{6}{16}$ and $\frac{8}{16}$)], a desired frequency characteristic can be obtained with steps of maximum 2 dB gain difference at the centre frequencies.

The sum of the filter outputs is fed through a coring circuit with a user definable transfer curve between −7 and +7 LSB at a 12-bit level. The definition of the coring LUT is realized with two control registers. Herein, for each of the points in the transfer curve, the user can define an output between 0 and the input value. For the LUT points +7 (and −7), a choice can be made from (−4) +4 to (−7) +7. By setting control bit CORING to LOW, the coring transfer curve is switched to a coarse coring which is only dependent on the threshold (see Fig.13).

The so formed peaking signal can be added to the original luminance signal, the sum of which then becomes the 9-bit output signal (black-to-white), with an additional DA shift fitting within 10 bits.

For dynamic use of the peaking circuit, an additional gain is provided on the peaking signal. This gain is made dependent on the energy in the peaking signal.

To overcome an unwanted coring on structured small signals, the output of the low-pass filter is also used to monitor if the high frequency contents are large enough to refrain from coring. Therefore the coring is set off if the HF energy level rises above a user definable threshold.

Spectral measurements are performed with the spectr_meas subpart, by calculating the sum of the absolute values from a chosen one of the three (high-pass and band-pass) filter outputs over a vertical window in a video field. With this window it is possible to disable subtitles. The maximum value of the chosen filter output within a windowed video field is also monitored. For the generally lower HF contents of the video signal, a weighting by a factor 4 can be switched in, while measuring on the High-Pass Filter (HPF).

7.2.18 NON-LINEAR PHASE FILTER BEFORE DAC

This non-linear phase filter adjusts for possible group delay differences in the Y, U and V output channels, and for sinus x/x bandwidth loss of the ADCs. The filter coefficients are $[-L \times (1 - u); 1 + L; -L \times u]$; where L determines the strength of the filter and u determines the asymmetry. The effect of the asymmetry is that for higher frequencies the delay is decreased for $u \leq 0.5$. Settings are provided for L = 0, $\frac{1}{8}$, $\frac{2}{8}$, $\frac{3}{8}$ and u = 0, $\frac{1}{4}$, $\frac{1}{2}$.

7.2.19 DCTI

The Digital Colour Transient Improvement (DCTI) is intended for U and V signals originating from a 4 : 1 : 1 source. Horizontal transients are detected and enhanced without overshoots by differentiating, making absolute and again differentiating the U and V signals separately. This signal is used as a pointer to make a time modulation.

This results in a 4 : 4 : 4 U and V bandwidth. To prevent third harmonic distortion, typical for this processing, a so called ‘over the hill protection’ prevents peak signals from becoming distorted. It is possible to control gain, width, connect U and V and over the hill range via the microcontroller.

At the output of the DCTI a post-filter is situated to make a correction for the simple upsampling in DCTI which is a linear interpolation [1; 2; 1]. The post-filter coefficients are [−1; 2; 6; 2; −1], convolution of both filters gives [−1; 0; 9; 16; 9; 0; −1]. This post-filter should only be used when the DCTI is off, and the source material is 4 : 2 : 2 bandwidth.

7.2.20 BORDER BLANK

The border and blanking processing is operating at a 4 : 4 : 4 level, just before the analog-to-digital conversion. Here it is possible to generate a blanking window and within this window a border window. The blanking window is used to blank the non-visible part of the output to the clamp level. The border window is the visible part of the video that contains no video, such as the sides in compression mode, this part can be programmed to display any luminance or colour level in an 8-bit accuracy; pixel repetition is also possible here. In case of multi PIP this block can generate separation borders in the horizontal and vertical direction.

7.3 Analog output blocks

7.3.1 Triple 10-bit digital-to-analog conversion

Three identical DACs are used to convert Y, U and V with a 32 or 16 MHz data rate.

7.3.2 Analog anti-aliasing post-filter

A 3rd-order linear phase filter is applied to each of the Y, U and V channels. It provides a notch on f_{clk} (32 MHz at Y, U and V) to strongly prevent aliasing to low frequencies, which would be most disturbing. The filters can be bypassed if external filtering with other characteristics is desired. Bandwidth and gain accuracy are given in Chapter 11.

7.3.3 PLL

The PLL consists of a ring oscillator, Discrete Time Oscillator (DTO) and digital control loop. The PLL characteristic is controlled by means of the microcontroller.

7.3.4 SNERT

A SNERT interface is built-in to transform the parallel data from the microcontroller into 1 or 2 Mbaud switchable SNERT data. This interface is also capable of reading data from the SNERT bus should it be required to access read registers.

The read or write operation must be set by the microcontroller. When writing to the bus, 2 bytes are loaded by the microcontroller; one for the address, the other for the data. When reading from the bus, 1 byte is loaded by the microcontroller for the address, the received byte is the data from the addressed SNERT location.

The SNERT interface replaces the standard UART interface. In contrast to the 80C51 UART interface there are additional control registers, other I/O pads and no byte separation time between address and data. After power-on reset the 1 Mbaud mode is active. Switching baud rate during transmission should be avoided.

7.3.5 PSP

For dynamically changing data such as timing signals, the programmable signal positioner generates them on the basis of parameters sent by the microcontroller. For the reset function of the microcontroller, a watchdog timer is also built-in that creates a reset pulse unless it is triggered by a change in the Bone signal within a preset time (1.05 s).

7.3.6 Microcontroller

The SAA4978H contains an embedded 80C51 microcontroller core including a 1 kbyte RAM and a 32 kbyte ROM. It also includes an I^2C-bus user control interface. For development reasons an external ROM can be accessed with 64 kbyte maximum size. An external emulator can be connected.

The main difference to most existing 80C51 derivatives is:

- 768 byte auxiliary RAM from which 128 bytes can be accessed as subtitle RAM
- Interrupt vector address for the I^2C-bus is 33H
- On-chip ROM code protection
- SNERT at 1 or 2 Mbaud with additional Sample Frequency Registers (SFRs) instead of UART
- Host interface containing all control registers access e.g. via MOVX instruction.

7.3.7 Board level testability

Boundary scan test is implemented, according to *“IEEE standard 1149.1”*. The boundary scan affects all digital pins and will cover all connections from the SAA4978H to other ICs that are also equipped with BST. The connectivity of the analog YUV input/output pins can also be tested with the use of BST.

The digital outputs UVAL, UVA0, UVA1, UVA2, UVA3, YAL, UVCL, UVC0, UVC1, UVC2, UVC3, YCL, WEA, WEC and IEC can be set in 3-state mode if not connected in the application. This means that these outputs with index 0 to 3 are set in 3-state if 4 : 1 : 1 is chosen, and the outputs with index L are set in 3-state if 8 bits output is chosen.

7.3.8 Power-on reset

All digital blocks except PLL are reset by a HIGH level at the reset pin. Only the watchdog counter is reset by the falling edge of the reset pulse. The PLL needs no reset. The frequency guard generates a single reset pulse with a duration of 0.875 ms when the actual frequency enters the desired range of 14 to 18 MHz. If the frequency leaves this range then no reset pulse is generated.

8 CONTROL REGISTER DESCRIPTION

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
Clamp registers (clamp position in steps of one pixel, only first quarter of line available)													
CLAMP_START	300	write			X	X	X	X	X	X	X	X	clamp start position
CLAMP_STOP	301	write			X	X	X	X	X	X	X	X	clamp stop position
AGC													
AGC_GAIN_Y	302	write		X	X	X	X	X	X	X	X	X	set Y gain (–3 to +6 dB)
AGC_GAIN_U	303	write		X	X	X	X	X	X	X	X	X	set U gain (–3 to +6 dB)
AGC_GAIN_V	304	write		X	X	X	X	X	X	X	X	X	set V gain (–3 to +6 dB)
Overflow detection control													
YUV_SELECT	305	write									X	X	select ADC (Y, U, V, V)
OVERFLOW_11_HIGH	300	read	E		X	X	X	X	X	X	X	X	read HIGH byte level 11
OVERFLOW_11_LOW	301	read	E		X	X	X	X	X	X	X	X	read LOW byte level 11
OVERFLOW_10_HIGH	302	read	E		X	X	X	X	X	X	X	X	read HIGH byte level 10
OVERFLOW_10_LOW	303	read	E		X	X	X	X	X	X	X	X	read LOW byte level 10
OVERFLOW_01_HIGH	304	read	E		X	X	X	X	X	X	X	X	read HIGH byte level 01; underflow/overflow
OVERFLOW_01_LOW	305	read	E		X	X	X	X	X	X	X	X	read LOW byte level 01; underflow/overflow
Digital front-end													
DFRONTEND_CONTROLS1	306	write			X	X	X	X	X	X	X	X	
U_CLAMP_COR_FVAL										X	X	X	U clamp correction value (twos complement) used in external correction mode
V_CLAMP_COR_FVAL							X	X	X				V clamp correction value (twos complement) used in external correction mode
UV_COR_MODE					X	X							UV clamp correction mode (internal, external, keep, keep)
DFRONTEND_CONTROLS2	307	write				X	X	X	X	X	X	X	
UV_TAU											X	X	select UV clamp time constant (4, 9, 19 and 39 lines)
Y_DELAY									X	X			select Y delay (–1, 0, 1, 2)

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
MFF_WIDTH						X	X	X					select MFF width (0, 3, 5, 7, 9, 9, 9 and 9 samples)
DFRONTEND_CONTROLS3	308	write						X	X	X	X	X	
NLP_L_AD											X	X	input λ settings (0, 1⁄16, 2⁄16, 3⁄16)
NLP_U_AD									X	X			input μ settings (0, 1⁄4, 1⁄2, 1⁄2)
NOTCH								X					select notch (off, on)
ACT_VIDEO_WINDOW_H_START	309	write			X	X	X	X	X	X	X	X	
ACT_VIDEO_WINDOW_H_LENGTH	30A	write			X	X	X	X	X	X	X	X	
ACT_VIDEO_WINDOW_V_START	30B	write		X	X	X	X	X	X	X	X	X	
ACT_VIDEO_WINDOW_V_LENGTH	30C	write	S	X	X	X	X	X	X	X	X	X	not double buffered for PSP (WEA)
CLAMP_U_ERROR	306	read			0	X	X	X	X	X	X	X	clamp offset in U (twos complement; gain 16) used in internal correction mode
CLAMP_V_ERROR	307	read			0	X	X	X	X	X	X	X	clamp offset in V (twos complement; gain 16) used in internal correction mode
Bus A output control													
BUS_A_CONTROL1	30D	write			X	X	X	X	X	X	X	X	
Y_BUS_A_8BIT_ROUND											X	X	Y bus A (9-bit rounded, 9-bit rounded, 8-bit dithered, 8-bit truncated)
Y_BUS_A_DITHER								X	X	X			dithering mode on Y bus A (F1L1, F1L2, F1L1,F1L2, F2L1, F2L2, F4L1, F4L2)
SEL_422_OUT							X						select 4 : 2 : 2 output format (4 : 1 : 1, 4 : 2 : 2)
UV_CORING					X	X							select UV coring mode (off, 0.5, 1.0, 1.5 LSB)
BUS_A_CONTROL2	30E	write				X	X	X	X	X	X	X	
UV_BUS_A_8BIT_ROUND											X	X	UV bus A (9-bit rounded, 9-bit rounded, 8-bit dithered, 8-bit rounded)
UV_BUS_A_DITHER								X	X	X			dithering mode on UV bus A (F1L1, F1L2, F1L1, F1L2, F2L1, F2L2, F4L1, F4L2)

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
FORCE_BUS_A_TRI							X						force bus A output to 3-state including WEA (off, on)
WE_A_QUALIFIER						X							WEA definition (prequalifier, qualifier)
Bus B input control													
BUS_B_CONTROL	30F	write				X	X	X	X	X	X	X	
SEL_INPUT_FORMAT											X	X	select input format (4 : 2 : 2 external, 4 : 1 : 1 external, 4 : 2 : 2 internal, 4 : 2 : 2 internal)
SEL_DOUBLE_CLOCK										X			select double input data rate (single, double clock)
SEL_ASYNCHRONOUS									X				select asynchronous input clock (synchronous, asynchronous clock)
UV_INV								X					invert U and V data (not inverted, inverted)
WE_B_QUALIFIER							X						WEB definition (prequalifier, qualifier)
INV656						X							invert MSB of bus B input (related to 656 based input)
TBC/SRC control													
C0	310	write	S	X	X	X	X	X	X	X	X	X	control of compression/expansion at line centre (twos complement: −256 to +255)
C2	311	write	S		X	X	X	X	X	X	X	X	control of compression/expansion at line edges (twos complement: −128 to +127)
H_SHIFT_HIGH	312	write	S		X	X	X	X	X	X	X	X	horizontal shift (bits 15 to 8)
H_SHIFT_LOW	313	write	S		X	X	X	X	X	X	X	X	horizontal shift (bits 7 to 0)
H_DATAPATH_DELAY	314	write	S		X	X	X	X	X	X	X	X	horizontal data path delay (bits 7 to 0)
H_DATAPATH_DELAY_SKEW	315	write	S			X	X	X	X	X	X	X	
H_DATAPATH_DELAY_MSB								X	X	X	X	X	horizontal data path delay (bits 12 to 8)
SKEW_MULT						X	X						skew multiply factor (off, 1, undefined, −1)

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
Noise estimator													
LIMERIC_THR_UP	316	write			X	X	X	X	X	X	X	X	threshold to define the weight factor of considered pixels
LIMERIC_WANTED_VALUE	317	write	S		X	X	X	X	X	X	X	X	sensitivity of noise estimator
LIMERIC_TASTE_AND_COMP	318	write	S		X	X	X	X	X	X	X	X	
TASTE_VALUE									X	X	X	X	taste value
COMPENSATION_VALUE					X	X	X	X					compensation value (twos complement)
LIMERIC_LB_DETAIL	319	write	S		X	X	X	X	X	X	X	X	bottom limit of detail counter
LIMERIC_UB_DETAIL	31A	write	S		X	X	X	X	X	X	X	X	top limit of detail counter
LIMERIC_YP_AND_OVLPL	31B	write	S		X	X	X	X	X	X	X	X	
OVERLAP_VALUE									X	X	X	X	overlap level for noise estimator (0 to 15)
PREFILTER_SCALING							X	X					luminance prefilter scaling (1, $\frac{1}{2}$, $\frac{1}{4}$, off)
SOB_NEGLECT						X							neglects the Sum Over a Block value of those blocks that contain values towards black and white; (use, neglect) = (measure except around black and white level, measure everywhere
INPUT8BIT					X								number of bits at input of NE block (9, 8)
NEST	308	read	E		0	0	0	0	X	X	X	X	noise estimator value
NEST_FILT	309	read	E		X	X	X	X	X	X	X	X	filtered noise estimator value
DETAIL_CNT_H	30A	read	E		X	X	X	X	X	X	X	X	number of details detected in field (HIGH byte)
DETAIL_CNT_L	30B	read	E		X	X	X	X	X	X	X	X	number of details detected in field (LOW byte)

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
Clamp noise reduction (CLINIC) control													
CLINIC_CONTROL	31C	write	S				X	X	X	X	X	X	
K_SCALE										X	X	X	select K scale (4, 2, 1, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$)
K_ONE									X				select K is 1 versus adaptive (adaptive, K = 1)
CLINIC_OFF								X					CLINIC function off (on, off)
DITHER							X						dither on (off, on)
CLINIC_MAX_DIFF	31D	write	S		X	X	X	X	X	X	X	X	maximum difference allowed between actual and stored segment value (bits 9 to 2)
CLINIC_THRESHOLD	31E	write	S		X	X	X	X	X	X	X	X	threshold to define motion in segments (bits 9 to 2)
CLINIC_DIF_AND_THR_LSB	31F	write	S						X	X	X	X	
MAX_DIFF_LSB											X	X	maximum difference allowed between actual and stored segment value (bits 1 and 0)
THRESHOLD_LSB									X	X			threshold to define motion in segments (bits 1 and 0)
NBR_EVENTS	30C	read	E		X	X	X	X	X	X	X	X	number of events per field with motion above threshold
TOT_COR_H	30D	read	E		X	X	X	X	X	X	X	X	accumulated absolute clamp correction in field (bits 18 to 11)
TOT_COR_M	30E	read	E		X	X	X	X	X	X	X	X	accumulated absolute clamp correction in field (bits 10 to 3)
TOT_COR_L	30F	read	E		0	0	0	0	0	X	X	X	accumulated absolute clamp correction in field (bits 2 to 0)
Line memory and noise reduction (LIMERIC) control													
LIMERIC_CONTROL	320	write	S		X	X	X	X	X	X	X	X	
N_DIST											X	X	select n_dist (2, 4, 8, 9)
PC_DIST									X	X			select pc_dist (1, 2, 3, 4)
PE_DIST							X	X					select pe_dist (5, 6, 7, 8)

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
WEAVE						X							weave on (off, on)
SEL_N_THR					X								select threshold from estimator versus threshold from microcontroller (estimator, microcontroller)
Band split peaking and coring													
PEAKING_CONTROL1	321	write	S		X	X	X	X		X	X	X	
2D_PEAK_COEF										X	X	X	2D peaking coefficient (0, $^{2}/_{4}$, $^{3}/_{4}$, $^{4}/_{4}$, $^{5}/_{4}$, $^{6}/_{4}$, $^{7}/_{4}$, $^{8}/_{4}$)
CORE_THR					X	X	X	X					coring threshold (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 LSB)
V_GAINSTR	322	write	S							X	X	X	vertical peaking (0, $^{1}/_{8}$, $^{2}/_{8}$, $^{3}/_{8}$, $^{4}/_{8}$, $^{5}/_{8}$, $^{6}/_{8}$, $^{7}/_{8}$)
Noise reduction energy measurement													
VHF_ENERGY_SUM_H	310	read	E		X	X	X	X	X	X	X	X	mean vertical energy measured in one field (bits 15 to 8)
VHF_ENERGY_SUM_L	311	read	E		X	X	X	X	X	X	X	X	mean vertical energy measured in one field (bits 7 to 0)
VHF_ENERGY_MAX	312	read	E		X	X	X	X	X	X	X	X	maximum vertical peak energy measured in one field
Black bar position and control													
BBD_FIRST_VIDEOLINE1	313	read	E		X	X	X	X	X	X	X	X	$^{1}/_{2}$ number of first line after black bar having video
BBD_LAST_VIDEOLINE1	314	read	E		X	X	X	X	X	X	X	X	$^{1}/_{2}$ number of last line before black bar having video
BBD_FIRST_VIDEOLINE2	315	read	E		X	X	X	X	X	X	X	X	$^{1}/_{2}$(number + 1) of first line after black bar having video
BBD_LAST_VIDEOLINE2	316	read	E		X	X	X	X	X	X	X	X	$^{1}/_{2}$(number + 1) of last line before black bar having video
BBD_WINDOW_H_START	323	write	S		X	X	X	X	X	X	X	X	
BBD_WINDOW_H_STOP	324	write	S		X	X	X	X	X	X	X	X	
BBD_WINDOW_V_START	325	write	S	X	X	X	X	X	X	X	X	X	
BBD_WINDOW_V_STOP	326	write	S	X	X	X	X	X	X	X	X	X	

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
BBD_LOGO_LENGTH	327	write	S		X	X	X	X	X	X	X	X	number of non-black samples permitted in a black bar line
BBD_SLICE_LEVEL1	328	write	S		X	X	X	X	X	X	X	X	½ threshold to detect black (detector 1)
BBD_SLICE_LEVEL2	329	write	S		X	X	X	X	X	X	X	X	½ threshold to detect black (detector 2)
Histogram control													
BLACK_OFFSET	32A	write	S		X	X	X	X	X	X	X	X	definition of DC shift in Y (twos complement)
LUT_DATA	32B	write			X	X	X	X	X	X	X	X	transfer of 32 bytes that define the Y transfer LUT from microcontroller to histogram (twos complement). The first write after a field reset resets the write pointer; subsequent write operations increment the write pointer.
THRESHOLD_HIS	32C	write	S		X	X	X	X	X	X	X	X	if $\lvert Y_n - Y_{n-1} \rvert$ > threshold then Y_n is added to the histogram
SPLIT_POSITION	32D	write	S		X	X	X	X	X	X	X	X	position of split point in steps of 4 pixels (left side unprocessed)
HISTOGRAM_CONTROL1	32E	write				X	X	X	X	X	X	X	not double buffered
HISTO_GAIN									X	X	X	X	histogram gain (0 to 15)
NOISE_RED								X					noise reduction on
FILTER_1_ON							X						1 : 2 : 1 filter on (off, on)
FILTER_2_ON						X							1 : 0 : 2 : 0 : 1 filter on (off, on)
RESERVED WRITE ADDRESS	32F	write											
YUV_IN_CONTROL	330	write	S				X	X	X		X	X	
ROUND												X	rounding versus truncating (truncated, rounded)
RATIO_LIMIT											X		select UV ratio 128 versus 64 (64, 128)
UV_POS									X				follow if dy > 0 versus follow dy (follow dy, follow if dy > 0)
UV_GAIN							X	X					UV gain (0, ½, 1, 2)
HGM_WINDOW_H_START	331	write	S		X	X	X	X	X	X	X	X	start of horizontal histogram window

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
HGM_WINDOW_H_STOP	332	write	S		X	X	X	X	X	X	X	X	stop of horizontal histogram window
HGM_WINDOW_V_START	333	write	S	X	X	X	X	X	X	X	X	X	start of vertical histogram window
HGM_WINDOW_V_STOP	334	write	S	X	X	X	X	X	X	X	X	X	stop of vertical histogram window
Histogram outputs													
HISTOGRAM_DATA	317	read			X	X	X	X	X	X	X	X	Histogram read command. The first read after a field reset resets the read pointer; subsequent read operations increment the read pointer.
Y_MIN	318	read	E		X	X	X	X	X	X	X	X	minimum Y value in previous field
Y_MAX	319	read	E		X	X	X	X	X	X	X	X	maximum Y value in previous field
U_MIN	31A	read	E		X	X	X	X	X	X	X	X	minimum U value in previous field
U_MAX	31B	read	E		X	X	X	X	X	X	X	X	maximum U value in previous field
V_MIN	31C	read	E		X	X	X	X	X	X	X	X	minimum V value in previous field
V_MAX	31D	read	E		X	X	X	X	X	X	X	X	maximum V value in previous field
MAX_HISTO_VALUE	31E	read	E		X	X	X	X	X	X	X	X	maximum value in histogram of previous field
SMART_BLACK	31F	read	E		X	X	X	X	X	X	X	X	black level indication (filtered Y_MIN)
Subtitle control													
THRESHOLD_HIGH	335	write			X	X	X	X	X	X	X	X	maximum level required for valid event
THRESHOLD_LOW	336	write			X	X	X	X	X	X	X	X	minimum level required for valid event
HIGH_TIME	337	write			X	X	X	X	X	X	X	X	minimum time above HIGH threshold required for valid event
LOW_TIME	338	write			X	X	X	X	X	X	X	X	minimum time below LOW threshold required for valid event
SUBTITLE_CONTROLS	339	write								X	X	X	
RESET_EVENTS												X	reset events (cumulative, reset)
EVENT_MODE											X		select event versus between thresholds mode (within thresholds, events)
RESET_PEAK										X			select ‘every field’ versus ‘bleed’ (bleed, every field)
SUBT_WINDOW_H_START	33A	write			X	X	X	X	X	X	X	X	

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
SUBT_WINDOW_H_STOP	33B	write			X	X	X	X	X	X	X	X	
SUBT_WINDOW_V_START	33C	write		X	X	X	X	X	X	X	X	X	
SUBT_WINDOW_V_STOP	33D	write		X	X	X	X	X	X	X	X	X	
EVENTS	280 to 2FF	read			X	X	X	X	X	X	X	X	Events read command. Number of transitions in the 128 lines of the subtitle window.
RESERVED READ ADDRESS	320	read											
PEAK_Y	321	read	E		X	X	X	X	X	X	X	X	½ peak value of Y within the event window
Bars control													
BAR_ARRAY	33E	write			X	X	X	X	X	X	X	X	Bar array write command. The first write after a field reset resets the write pointer; subsequent write operations increment the write pointer (see also BAR_ARRAY_RESOLUTION).
BAR_ARRAY_Y	33F	write	S		X	X	X	X	X	X	X	X	display bar luminance level
BAR_ARRAY_U	340	write	S		X	X	X	X	X	X	X	X	display bar U level (twos complement)
BAR_ARRAY_V	341	write	S		X	X	X	X	X	X	X	X	display bar V level (twos complement)
BAR_ARRAY_H_START	342	write	S		X	X	X	X	X	X	X	X	horizontal start position of the display bars (see also BAR_ARRAY_RESOLUTION)
BAR_ARRAY_V_START	343	write	S		X	X	X	X	X	X	X	X	vertical start position of the display bars
BAR_ARRAY_WIDTH	344	write	S		X	X	X	X	X	X	X	X	the width of each bar in number of lines (see also BAR_ARRAY_RESOLUTION)
BAR_ARRAY_SPACE	345	write	S		X	X	X	X	X	X	X	X	the number of lines between two bars (see also BAR_ARRAY_RESOLUTION)
BAR_ARRAY_CONTROL	346	write	S							X	X	X	
BAR_ARRAY_ON												X	select bar array on (off, on)

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
BAR_ARRAY_RESOLUTION											X		select bar array resolution (BAR_ARRAY_H_START × 4, BAR_ARRAY_WIDTH × 2, BAR_ARRAY_SPACE × 2, BAR_ARRAY × 4, BAR_ARRAY_H_START × 2, BAR_ARRAY_WIDTH × 1, BAR_ARRAY_SPACE × 1, BAR_ARRAY × 2)
BAR_ARRAY_TRANS										X			select mashing versus superimpose (superimpose, mashing)
Bus C output control													
BUS_C_CONTROL1	347	write	S		X	X	X	X	X	X	X	X	
SEL422OUT												X	select 4 : 2 : 2 output (4 : 1 : 1, 4 : 2 : 2) overridden by DPCM
UV_BUS_C_8BIT_ROUND										X	X		UV bus C (9-bit rounded, 9-bit rounded, 8-bit dithered, 8-bit truncated)
MPIP								X	X				multi-PIP mode (off, 2 × 2, 3 × 3, 4 × 4); see also memory write control
UV_BUS_C_DITHER					X	X	X						dither line and field phase (f1l1, f1l2, f1l1, f1l2, f2l1, f2l2, f4l1, f4l2)
BUS_C_CONTROL2	348	write	S			X	X	X	X	X	X	X	
DPCM												X	DPCM output (4 : 1 : 1/4 : 2 : 2, DPCM) overrides SEL422OUT
FORCE_BUS_C_TRI											X		force bus C to 3-state including WEC and IEC (off, on)
Y_BUS_C_8BIT_ROUND									X	X			Y bus C (9-bit rounded, 9-bit rounded, 8-bit dithered, 8-bit truncated)
Y_BUS_C_DITHER						X	X	X					dither line and field phase (f1l1, f1l2, f1l1, f1l2, f2l1, f2l2, f4l1, f4l2)

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
Field memory control													
WE_WINDOW_H_START	349	write			X	X	X	X	X	X	X	X	start of horizontal write enable window
WE_WINDOW_H_STOP	34A	write			X	X	X	X	X	X	X	X	stop of horizontal write enable window
ACQ_EN_WINDOW_V_START	34B	write		X	X	X	X	X	X	X	X	X	start of vertical write and input enable window
ACQ_EN_WINDOW_V_STOP	34C	write		X	X	X	X	X	X	X	X	X	stop of vertical write and input enable window
IE_WINDOW_H_START	34D	write			X	X	X	X	X	X	X	X	start of horizontal input enable window
IE_WINDOW_H_STOP	34E	write			X	X	X	X	X	X	X	X	stop of horizontal input enable window
WE_IE_SHIFT	34F	write							X	X	X	X	
WE_C_SHIFT											X	X	fine shift of WEC (0, 1, 2, 3 pixels)
IE_C_SHIFT									X	X			fine shift of IEC (0, 1, 2, 3 pixels)
CHOP_CYCLE	350	write									X	X	chop cycle of WEC and IEC (1, ½, ⅓, ¼)
RE_WINDOW_H_START	351	write			X	X	X	X	X	X	X	X	define start of horizontal read enable window
RE_WINDOW_H_STOP	352	write			X	X	X	X	X	X	X	X	define stop of horizontal read enable window
RE_WINDOW_V_START	353	write		X	X	X	X	X	X	X	X	X	define start of vertical read enable window
RE_WINDOW_V_STOP	354	write		X	X	X	X	X	X	X	X	X	define stop of vertical read enable window
Bus D input control													
BUS_D_CONTROL	355	write	S						X		X	X	
SEL_INPUT_FORMAT											X	X	select input format (4 : 2 : 2 external, 4 : 1 : 1 external, 4 : 2 : 2 internal, DPCM external)
UNDITHER									X				select undither active (off, on)
BE_WINDOW_H_START	356	write			X	X	X	X	X	X	X	X	
BE_WINDOW_H_STOP	357	write			X	X	X	X	X	X	X	X	
BE_WINDOW_V_START	358	write		X	X	X	X	X	X	X	X	X	
BE_WINDOW_V_STOP	359	write		X	X	X	X	X	X	X	X	X	

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
CTI control													
DBACKEND_CONTROLS1	35A	write			X	X	X	X	X	X			
CTI_SEPARATE										X			separate U and V processing (linked, separate)
CTI_PROTECTION									X				select hill protection (off, on)
CTI_GAIN						X	X	X					CTI gain (0, $\frac{1}{8}$, $\frac{2}{8}$, $\frac{3}{8}$, $\frac{4}{8}$, $\frac{5}{8}$, $\frac{6}{8}$, $\frac{7}{8}$)
CTI_FILTER_ON					X								post-filter on (off, on)
DBACKEND_CONTROLS2	35B	write			X	X	X	X	X	X	X	X	
CTI_LIMIT											X	X	limit CTI range (0, ±4, ±8, ±12)
CTI_SUPERHILL										X			select super hill protection (off, on)
CTI_DDX_SEL									X				select first differentiating filter (–1 0 0 1, –1 –2 –1 1 2 1)
CTI_SUPERHILL					X	X	X	X					hill detection threshold (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)
NLP_DA	35C	write							X	X	X	X	
NLP_L_DA											X	X	output λ settings (0, $\frac{1}{8}$, $\frac{2}{8}$, $\frac{3}{8}$)
NLP_U_DA									X	X			output μ settings (0, $\frac{1}{4}$, $\frac{1}{2}$, $\frac{1}{2}$)
Dynamic peaking and coring													
PEAKING_CONTROL2	35D	write	S		X	X	X	X	X	X	X	X	
ALPHA										X	X	X	α value (0, $\frac{1}{16}$, $\frac{2}{16}$, $\frac{3}{16}$, $\frac{4}{16}$, $\frac{5}{16}$, $\frac{6}{16}$, $\frac{8}{16}$)
BETA							X	X	X				β value (0, $\frac{1}{16}$, $\frac{2}{16}$, $\frac{3}{16}$, $\frac{4}{16}$, $\frac{5}{16}$, $\frac{6}{16}$, $\frac{8}{16}$)
DELTA					X	X							δ value (0, $\frac{1}{4}$, $\frac{1}{2}$, 1)
LUTREGA	35E	write	S		X	X	X	X	X	X	X	X	programmable coring replacement values for luminance levels 1 to 4
LEVEL1												X	level 1 (0, 1)
LEVEL2										X	X		level 2 (0, 1, 2, 3)
LEVEL3								X	X				level 3 (0, 1, 2, 3)
LEVEL4					X	X	X						level 4 (0, 1, 2, 3, 4, 5, 6, 7)
LUTREGB	35F	write	S		X	X	X	X	X	X	X	X	programmable coring replacement values for luminance levels 5 to 7

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
LEVEL5										X	X	X	level 5 (0, 1, 2, 3, 4, 5, 6, 7)
LEVEL6							X	X	X				level 6 (0, 1, 2, 3, 4, 5, 6, 7)
LEVEL7					X	X							level 7 (4, 5, 6, 7)
COR_THR	360	write	S		X	X	X	X	X	X	X	X	local energy above coring-threshold switches off coring
PEAKING_CONTROL3	361	write	S		X	X	X	X	X	X	X	X	
TAU										X	X	X	τ value ($0, {}^{1}/_{16}, {}^{2}/_{16}, {}^{3}/_{16}, {}^{4}/_{16}, {}^{5}/_{16}, {}^{6}/_{16}, {}^{8}/_{16}$)
NEGGAIN								X	X				negative gain value ($0, {}^{1}/_{4}, {}^{1}/_{2}, 1$)
CORING							X						coring (coarse, fine) in accordance with LUTREGA and LUTREGB; see Fig.13
ENERGY_SEL					X	X							energy select (high $\times$ 4, mid, low, high)
ENERGY_SELECT_V_START	362	write		X	X	X	X	X	X	X	X	X	start of vertical energy select window
ENERGY_SELECT_V_STOP	363	write		X	X	X	X	X	X	X	X	X	stop of vertical energy select window
RESERVED READ ADDRESS	322	read	E		X	X	X	X	X	X	X	X	
RESERVED READ ADDRESS	323	read	E		X	X	X	X	X	X	X	X	
ENERGY_MAX	324	read	E		X	X	X	X	X	X	X	X	maximum peak energy measured in one field
Blanking control (definition of blanking window)													
BLANKING_WINDOW_H_START	364	write			X	X	X	X	X	X	X	X	
BLANKING_WINDOW_H_STOP	365	write			X	X	X	X	X	X	X	X	
BLANKING_WINDOW_V_START	366	write		X	X	X	X	X	X	X	X	X	
BLANKING_WINDOW_V_STOP	367	write		X	X	X	X	X	X	X	X	X	
Border control													
BORDER_SIDE_H_START	368	write			X	X	X	X	X	X	X	X	start of right border
BORDER_SIDE_H_STOP	369	write			X	X	X	X	X	X	X	X	end of left border
BORDER_SIDE_V_START	36A	write		X	X	X	X	X	X	X	X	X	start of lower border
BORDER_SIDE_V_STOP	36B	write		X	X	X	X	X	X	X	X	X	stop of upper border
BORDER_BAR_H_START	36C	write			X	X	X	X	X	X	X	X	start of first horizontal bar
BORDER_BAR_H_WIDTH	36D	write			X	X	X	X	X	X	X	X	width of horizontal bars
BORDER_BAR_V_START	36E	write		X	X	X	X	X	X	X	X	X	start of first vertical bar

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
BORDER_BAR_V_WIDTH	36F	write		X	X	X	X	X	X	X	X	X	width of vertical bars
BORDER_REPEAT_H	370	write			X	X	X	X	X	X	X	X	horizontal repeat value
BORDER_REPEAT_V	371	write		X	X	X	X	X	X	X	X	X	vertical repeat value
BORDER_Y	372	write			X	X	X	X	X	X	X	X	Y value of sides and bars
BORDER_U	373	write			X	X	X	X	X	X	X	X	U value of sides and bars (twos complement)
BORDER_V	374	write			X	X	X	X	X	X	X	X	V value of sides and bars (twos complement)
PLL													
PLL_CK_AND_CD	375	write	V		X	X	X	X	X	X	X	X	
PLL_CK			V					X	X	X	X	X	K factor control (0 to 31)
PLL_CD			V		X	X	X						damping control (0 to 7)
PLL_IDTO_PLUS_VARIOUS	376	write				X	X	X		X	X	X	
PLL_IDTO(18-16)			V							X	X	X	increment offset for DTO bits 18 to 16 (twos complement; bit 18 is the sign bit)
PLL_OFF								X					PLL off; keep output frequency (off, on)
PLL_OPEN			V				X						PLL open loop mode (closed, open)
DO_SNAP						X							do snapshot
PLL_IDTO(15-8)	377	write	V		X	X	X	X	X	X	X	X	increment offset for DTO bits 15 to 8
PLL_IDTO(7-0)	378	write	V		X	X	X	X	X	X	X	X	increment offset for DTO bits 7 to 0; transfers all bits (18 to 0)
PLL_SKEW_DELAY	379	write								X	X	X	skew transferred: 512 × (1 + PLL_SKEW_DELAY) clocks after HREF; PLL_SKEW_DELAY (0 to 7)
PLL_PE_MAX(15-8)	325	read	V		X	X	X	X	X	X	X	X	maximum phase offset during field HIGH byte
PLL_PE_MAX(7-0)	326	read	V		X	X	X	X	X	X	X	X	maximum phase offset during field LOW byte; transfers all bits (15 to 0)
PLL_PE_MIN(15-8)	327	read	V		X	X	X	X	X	X	X	X	minimum phase offset during field HIGH byte

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
PLL_PE_MIN(7-0)	328	read	V		X	X	X	X	X	X	X	X	minimum phase offset during field LOW byte; transfers all bits (15 to 0)
PLL_PE_SUM(15-8)	329	read	V		X	X	X	X	X	X	X	X	accumulated phase offset during field HIGH byte
PLL_PE_SUM(7-0)	32A	read	V		X	X	X	X	X	X	X	X	accumulated phase offset during field LOW byte; transfers all bits (15 to 0)
PLL_PE_SABS(15-8)	32B	read	V		X	X	X	X	X	X	X	X	accumulated absolute phase offset during field HIGH byte
PLL_PE_SABS(7-0)	32C	read	V		X	X	X	X	X	X	X	X	accumulated absolute phase offset during field LOW byte; transfers all bits (15 to 0)
PLL_INC_OFFSET(19-16)	32D	read	V		0	0	0	0	X	X	X	X	increment offset bits 19 to 16 (twos complement; bit 19 is the sign bit)
PLL_INC_OFFSET(15-8)	32E	read	V		X	X	X	X	X	X	X	X	increment offset bit HIGH byte
PLL_INC_OFFSET(7-0)	32F	read	V		X	X	X	X	X	X	X	X	increment offset bit LOW byte; transfers all bits (19 to 0)
PLL_CKA_VALUE	330	read	V		0	0	0	X	X	X	X	X	actual K value
PLL_ADAPT_STATUS	331	read	V		0	0	0	0	0	0	0	X	PLL adaptive status (locked, unlocked)
RESERVED READ ADDRESS	332	read											
Read registers PSP													
HA_VALUE	333	read			X	X	X	X	X	X	X	X	available after VA or COPY_VALUE_STROBE
VA_VALUE	334	read			X	X	X	X	X	X	X	X	as HA_VALUE; bit 8 in register VARIOUS_BITS
HD_VALUE	335	read			X	X	X	X	X	X	X	X	available after VD or COPY_VALUE_STROBE
VD_VALUE	336	read			X	X	X	X	X	X	X	X	as HD_VALUE; bit 8 in register VARIOUS_BITS
PIP_RISING_EDGE_POS	337	read			X	X	X	X	X	X	X	X	
PIP_FALLING_EDGE_POS	338	read			X	X	X	X	X	X	X	X	
INTR_0_SOURCE	339	read			0	0	0	0	0	0	X	X	interrupt read; **register reset after read**

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
VA_INTR_ACTIVE												X	VA interrupt active (not active, active)
WE_INTR_ACTIVE											X		WE interrupt active (not active, active)
VARIOUS_BITS	33A	read			0	0	0	0	0	0	X	X	
VA_VALUE_MSB												X	MSB of VA
VD_VALUE_MSB											X		MSB of VD
Various PSP control													
VA_SYNC_WINDOW_START	37A	write		X	X	X	X	X	X	X	X	X	start of vertical VA_SYNC enable window
VA_SYNC_WINDOW_STOP	37B	write		X	X	X	X	X	X	X	X	X	stop of vertical VA_SYNC enable window
VA_INC_HOR_POS	37C	write			X	X	X	X	X	X	X	X	horizontal position of VA_COUNTER clock
HREF_EXT_START	37D	write			X	X	X	X	X	X	X	X	start HREFEXT pulse
HREF_EXT_STOP	37E	write			X	X	X	X	X	X	X	X	stop HREFEXT pulse
INTR_AND_SYNC_ENABLE	37F	write			X	X	X			X	X	X	
INTR_VA_ENABLE												X	VA interrupt enable (disabled, enabled)
INTR_WE_ENABLE											X		WE interrupt enable (disabled, enabled)
INTR_VD_ENABLE										X			VD interrupt enable (disabled, enabled)
HD_CNTR_RST_BY_HDREF							X						HD counter reset from HD_REF (no reset, reset by HD_REF)
DIVIDE_VD_INC						X							divide VD_INC by 2 (100 Hz, progressive scan mode)
SEL_HA_CLAMP					X								select clamp-counter reset (HA_REF, HA)
INTR_VA_DELAY	380	write		X	X	X	X	X	X	X	X	X	delay in number of lines delay at pin 157 caused by VA
HD_START	381	write			X	X	X	X	X	X	X	X	start HD pulse
HD_STOP	382	write			X	X	X	X	X	X	X	X	stop HD pulse
VD_HOR_POS	383	write			X	X	X	X	X	X	X	X	horizontal phase of VD
H_EXT_POS	384	write			X	X	X	X	X	X	X	X	HD counter length

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
INTR_VD_DELAY	385	write		X	X	X	X	X	X	X	X	X	value of COUNTER_VD that initiates interrupt 1
PLL_OFF_START	386	write		X	X	X	X	X	X	X	X	X	vertical start of PLL_OFF window
PLL_OFF_STOP	387	write		X	X	X	X	X	X	X	X	X	vertical stop of PLL_OFF window
DISPLAY_CONTROL	388	write			X	X	X	X	X	X	X	X	
RE_SHIFT											X	X	RE pixel shift (0, 1, 2, 3)
ENABLE_RESET_BLANK										X			enable blank reset (disabled, enabled)
PIXEL_REPETITION									X				enable pixel repetition (disabled, enabled)
ENABLE_BORDER_V_BAR								X					enable vertical bars (disabled, enabled)
ENABLE_BORDER_V_SIDE							X						enable vertical sides (disabled, enabled)
ENABLE_BORDER_H_BAR						X							enable horizontal bars (disabled, enabled)
ENABLE_BORDER_H_SIDE					X								enable horizontal sides (disabled, enabled)
RESERVED WRITE ADDRESS	389	write											
ACQ_WINDOWS_RESET	38A	write											TRIGGER to reset acquisition windows
COPY_VALUE_STROBE	38B	write											TRIGGER to copy register values
TRIGGER_FLYBACK	38C	write											TRIGGER to set VD output
TRIGGER_SCAN	38D	write											TRIGGER to reset VD output
COUNTER_VD_RESET	38E	write											TRIGGER to reset VD counter
INTR_1_RESET	38F	write											TRIGGER to reset interrupt 1
DISPLAY_WINDOWS_RESET	390	write											TRIGGER to reset display windows
SEL_1FH	391	write										X	select back-end clock at 16 MHz for $1f_H$ processing (32 MHz, 16 MHz)
BUS_B_VREF	392	write		X	X	X	X	X	X	X	X	X	vertical start field reference for bus B
NRPXDIV4	393	write	S		X	X	X	X	X	X	X	X	$\frac{1}{4}$ of horizontal length of video data in data path

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
Testing													
RESET_CONTROL	394	write										X	
FIELD_RESET												X	
TEST_Y_IN_D	33B	read			X	X	X	X	X	X	X	X	test receive register at bus D; Y input
TEST_UV_IN_D	33C	read			X	X	X	X	X	X	X	X	test receive register at bus D; UV input
Analog blocks													
ANASWITCH	395	write			X	X	X	X	X	X	X	X	test register for analog functions; normal application mode: 49H
CLAMP_ACTIVE												X	clamp active
STDIFF_CONV											X		single to differential converter
STDIFF_CONV_AGC										X			single to differential converter and AGC
STDIFF_CONV_AGC_FILTER									X				single to differential converter, AGC and filter
FRONTEND_TO_OUTPUT								X					front-end to output
ATT_OUT							X						attenuator to output
ATT_RECONSTRUCT_OUT						X							attenuator and reconstruction filter to output
FRONTEND_TO_BACKEND					X								front-end to back-end
RESERVED WRITE ADDRESS	396	write							X	X	X	X	
RESERVED WRITE ADDRESS	397	write										X	
TM_AD_DA	398	write								X	X	X	test mode AD, DA blocks
TM_ADDA2												X	ADC and DAC test
TM_ADDA1											X		ADC and DAC test
TM_AD2DA										X			direct bypass from ADC to DAC

NAME	ADDRESS HEX	READ/ WRITE	DOUBLE BUFFERED[1]	8	7	6	5	4	3	2	1	0	DESCRIPTION
SNERT control (these registers are implemented as special function register, they have a HEX address outside the normal control register range)													
SNCON	98	read/ write			X	0	0	0	0	0	X	X	SNERT control register (reset on bit 1 of register $E8: power-on reset)
TRM		read										X	SNERT transmit busy flag
REC		read/ write									X		SNERT receive busy flag
MB2		read/ write			X								SNERT baud rate (1 MHz, 2 MHz)
SNADD	99	write			X	X	X	X	X	X	X	X	address of SNERT message to be transmitted
SNWDA	9A	write			X	X	X	X	X	X	X	X	data of SNERT message to be transmitted
SNRDA	9B	read			X	X	X	X	X	X	X	X	data from SNERT bus after a completed reception

Note

1. Blank means not double buffered; E means double buffered and data available at end of active video; S means double buffered and data clocked in at start of active video; V means double buffered and data valid at start of VA.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	–0.5	+6	V
V_{DDD}; V_{DDO}	digital supply voltage	–0.5	+6	V
$\Delta V_{DDA - DDD}$	supply voltage difference between analog and digital supply voltages	–0.5	+0.5	V
$\Delta V_{DDA - DDO}$	supply voltage difference between analog and output supply voltages	–0.5	+0.5	V
V_I	input voltage for all digital input and digital I/O pins	–0.5	+5.5	V
V_i	analog input voltage	–0.3	V_{DDA} + 0.3	V
T_{stg}	storage temperature	–55	+150	°C
T_j	operating junction temperature	0	125	°C

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	25	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		2	K/W

11 CHARACTERISTICS

V_{DDD} = V_{DDA} = 3.3 V; AGC at 0 dB; T_{amb} = 25 °C; nominal parameter settings: $2f_H$/100 Hz mode; features transparent; equalized frequency response test signal: EBU colour bar 100/0/75/0 *"CCIR471-1"*; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
$V_{DD(I/O)}$	microcontroller I/O supply voltage		3.0	–	5.5	V
V_{DDO}	digital supply voltage for outputs		3.0	3.3	3.6	V
Dissipation						
P_{tot}	total power dissipation		–	–	1.6	W
YUV input processing (including AGC)						
Y_{AGC}	Y AGC setting to obtain full ADC range	$V_{i(Y)(b-w)}$ = 1.0 V (p-p); note 1	117	132	148	–
U_{AGC}	U AGC setting to obtain full ADC range	$V_{i(U)}$ = 1.33 V (p-p); note 1	120	136	151	–
V_{AGC}	V AGC setting to obtain full ADC range	$V_{i(V)}$ = 1.05 V (p-p); note 1	117	132	148	–
$\Delta E_{G(YUV)all}$	overall input to output gain error between Y, U and V	f = 0 to 2.5 MHz (analog filters off)	–5.6	–	+5.6	%
$\Delta E_{G(UV)i}$	gain error between U and V inputs	f = 0 to 2.5 MHz (analog filters off) from input to digital domain	–	1	3.2	%
$\Delta E_{G(UV)all}$	overall gain error between U and V	f = 0 to 2.5 MHz (analog filters off) from input to output	–	1.2	4.0	%
$\Delta E_{G(f)(UV)i}$	filtered gain error between U and V input	f = 0 to 1.25 MHz (analog filters on) from input to digital domain	–	2	6.4	%
$\Delta E_{G(f)(UV)all}$	overall filtered gain error between U and V	f = 0 to 2.5 MHz (analog filters on) from input to output	–	2.5	8	%
C_i	input capacitance		–	7	15	pF
I_{LI}	input leakage current	clamp not active; $0 < V_i < V_{DDA} + 0.3$	–	–	100	nA
$\Delta G_{AGC(min-max)}$	difference in gain between AGC minimum and maximum		9	9.5	10	dB
$G_{AGC(acc)}$	AGC gain accuracy digital		–	9	–	bits
$G_{step(AGC)}$	step resolution gain of AGC	maximum gain variation per step	–	–	0.4	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{ct}	crosstalk between inputs and outputs	f = 0 to 1 MHz; Z_{source} = 200 Ω	–	–	50	dB
		f = 1 to 5 MHz; Z_{source} = 200 Ω	–	–	44	dB
Input clamp processing (Y clamp level digital 32; U and V clamp level digital 0 in twos complement)						
$E_{clamp(stat)(Y)}$	static clamp error in Y channel		–5.0	–	+2.0	LSB
$E_{clamp(stat)(UV)}$	static clamp error in UV channel	digital correction circuit off	–3.0	–	+3.0	LSB
$E_{clamp(dyn)}$	dynamic clamp error	average value (1 σ)	–	–	0.25	LSB
C_{clamp}	clamping capacitance		10	22	–	nF
R_{source}	source resistance		–	–	350	Ω
$I_{clamp(max)}$	maximum clamp current		–160	–	+160	μA
Tilt	maximum drift in one line period		–	–	0.25	LSB
$V_{i(clamp)(Y)}$	Y input clamping voltage	over complete AGC range	600	–	–	mV
Input transfer functions (sample rate 16 MHz; 9 bits); see Fig.7						
$f_{i(s)(max)}$	maximum input sample frequency		18	–	–	MHz
δ_{clk}	duty factor of (internal) clock cycle		40	–	60	%
INL	DC integral non linearity	ramp input signal; AGC on; filters off	–2	–	+2	LSB
DNL	DC differential non linearity	ramp input signal; note 2	–0.99	–	+0.99	LSB
SNR	overall signal-to-noise ratio (no harmonics) from input to output	note 3	50	52	–	dB
$\Phi_{diff(UV)}$	differential phase in U and V		–	1	2.5	deg
$G_{diff(Y)}$	differential gain in Y front-end	Y within 0.2 to 0.75 V	–	–	1.5	%
$\Phi_{diff(Y)}$	differential phase in Y front-end	Y within 0.2 to 0.75 V	–	–	1	deg
SVRR	supply voltage ripple rejection	filters off; note 4	35	–	–	dB
PLL function (base frequency 32 MHz)						
$\sigma_{line\text{-}line}$	sigma value of line-to-line jitter	locked to stable HA; note 5	–	0.4	1.0	ns
$\sigma_{field\text{-}field}$	sigma value of field-to-field jitter	locked to stable HA; note 5	–	0.4	1.0	ns
f_{unlock}	frequency in unlocked state		30.7	32	33.3	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV output processing; note 6; see Fig.6						
$V_{o(Y)(b-w)}$	Y black-to-white output voltage	Z_L = 10 kΩ	0.96	1.00	1.04	V
$V_{o(U)(p-p)}$	U output voltage (peak-to-peak value)	Z_L = 10 kΩ	1.27	1.33	1.38	V
$V_{o(V)(p-p)}$	V output voltage (peak-to-peak value)	Z_L = 10 kΩ	1.01	1.05	1.09	V
$\Delta E_{G(UV)o}$	gain error between U and V output	f = 0 to 2.5 MHz (analog filters off) from digital domain to output	–	–	2.5	%
$\Delta E_{G(f)(UV)o}$	filtered gain error between U and V output	f = 0 to 2.5 MHz (analog filters on) from digital domain to output	–	–	5	%
Z_o	output impedance	f = 0 to 10 MHz	65	75	85	Ω
$V_{Y(d)(0)}$	Y super black level voltage at 0	V_{bY} = black level voltage	V_{bY} – 0.63	V_{bY} – 0.6	V_{bY} – 0.57	V
$V_{Y(d)(1023)}$	Y super white (headroom) voltage at 1023	V_{bY} = black level voltage	V_{bY} + 1.47	V_{bY} + 1.53	V_{bY} + 1.59	V
$V_{Y(d)(288)}$	Y black level voltage at 288	V_{bY} = black level voltage	–	V_{bY}	–	V
$V_{Y(d)(768)}$	Y white level voltage at 768	V_{bY} = black level voltage	V_{bY} + 0.96	V_{bY} + 1.0	V_{bY} + 1.04	V
$V_{U(d)(0)}$	U voltage at 0	V_{bU} = lower U voltage; note 7	–	V_{bU}	–	V
$V_{U(d)(1023)}$	U voltage at 1023		V_{bU} + 1.43	V_{bU} + 1.49	V_{bU} + 1.55	V
$V_{V(d)(0)}$	V voltage at 0	V_{bV} = lower V voltage; note 7	–	V_{bV}	–	V
$V_{V(d)(1023)}$	V voltage at 1023		V_{bV} + 1.13	V_{bV} + 1.18	V_{bV} + 1.23	V
$\alpha_{res(clk)}$	residual clock attenuation related to YOUT	f = 32 or 16 MHz	–	–	40	dB
Output transfer functions (sample rate 32 MHz; 10 bits)						
$f_{clk(max)}$	maximum sample clock		33.4	–	–	MHz
δ_{clk}	duty factor of clock cycle		40	–	60	%
INL	DC integral non linearity		–2	–	+2	LSB
DNL	DC differential non linearity	note 2	–0.75	–	+0.75	LSB
Digital output bus A and C, WEA, WEC, IEC and HREFEXT (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ); timing referred to CLK16, HREFEXT is not a 3-state output						
V_{OH}	HIGH-level output voltage		2.4	–	–	V
V_{OL}	LOW-level output voltage		–	–	0.4	V
I_{OZ}	output current in 3-state mode	$-0.1 < V_o < V_{DDO} + 0.1$	–	–	1.0	μA
$V_{ext(OZ)}$	external applied voltage in 3-state mode		–	–	V_{DDO} + 0.3	V
$t_{d(o)}$	output delay time	see Fig.4	–	–	30	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{h(o)}$	output hold time	see Fig.4	4	–	–	ns
SR	slew rate		200	500	700	$\frac{mV}{ns}$
Digital input bus B and D; timing referred to CLK32 for bus D and to CLK16, CLK32 or CLKAS for bus B (see Fig.4)**; the reference for bus B depends on the selected mode respectively single clock, double clock or asynchronous clock**						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage	5 V tolerant	2.0	–	5.5	V
$t_{su(i)}$	input set-up time	see Fig.4	6	–	–	ns
$t_{h(i)}$	input hold time	see Fig.4	1	–	–	ns
CLKAS						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage	5 V tolerant	2.0	–	5.5	V
$t_{h(i)(async)}$	asynchronous input hold time		4	–	–	ns
$t_{L(min)}$	minimum LOW time		–	–	10	ns
$t_{H(min)}$	minimum HIGH time		–	–	10	ns
$T_{CLKAS(min)}$	minimum period time	the asynchronous clock may not be faster than CLK32	T_{CLK32}	–	–	ns
CLK16 and CLK32 (C_L = 30 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
V_{OL}	LOW-level output voltage		0	–	0.4	V
V_{OH}	HIGH-level output voltage		2.4	–	–	V
$t_{o(r)}$	output rise time	see Fig.4	2	3	4	ns
$t_{o(f)}$	output fall time	see Fig.4	2	3	4	ns
t_{dHO}	CLK16 HIGH transition delay time	see Fig.5	–	–	20	ns
t_{hHO}	CLK16 HIGH transition hold time	see Fig.5	4	–	–	ns
t_{dLO}	CLK16 LOW transition delay time	see Fig.5	–	–	20	ns
t_{hLO}	CLK16 LOW transition hold time	see Fig.5	4	–	–	ns
RED, HD and VD (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ); timing referred to CLK32; see Fig.4						
V_{OH}	HIGH-level output voltage		2.4	–	–	V
V_{OL}	LOW-level output voltage		–	–	0.4	V
$t_{d(o)}$	output delay time	see Fig.4	–	–	20	ns
$t_{h(o)}$	output hold time	see Fig.4	4	–	–	ns
SR	slew rate		200	500	700	$\frac{mV}{ns}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator stage (operation with crystal or external clock)						
f_{osc}	oscillator frequency		–	12	–	MHz
C_{L34}	recommended load capacitor	see Fig.11	–	12	–	pF
C_{L35}			–	18	–	pF
$R_{ser1(xtal)}$	crystal series resistance	see Fig.12	–	–	250	Ω
$C_{par(xtal)}$	crystal parallel capacitance	see Fig.12	–	–	7	pF
I²C-bus signal: SDA and SCL; note 8						
V_{IH}	HIGH-level input voltage		$0.7V_{DDIO}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDIO}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3.0 mA	–	–	0.4	V
f_{SCL}	SCL clock frequency		–	–	400	kHz
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
t_{SCLL}	SCL LOW time		1.3	–	–	µs
t_{SCLH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{SU;DAT1}$	data set-up time (before repeated START condition)		0.6	–	–	µs
$t_{SU;DAT2}$	data set-up time (before STOP condition)		0.6	–	–	µs
$t_{SU;STA}$	set-up time repeated START		0.6	–	–	µs
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs
SNERT bus timing valid for both 1 and 2 Mbaud: SNDA and SNCL; see Fig.10						
V_{OH}	HIGH-level output voltage	I_{OH} = –0.06 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
$t_{su(i)(SNCL)}$	input set-up time to SNCL		80	–	–	ns
$t_{h(i)(SNCL)}$	input hold time to SNCL		0	–	–	ns
$t_{h(o)}$	output hold time		50	–	–	ns
$t_{su(o)}$	output set-up time		260	–	–	ns
$t_{dis(o)}$	output disable time		–	–	200	ns
$t_{cy(SNCL)}$	SNCL cycle time		500	–	1000	ns
t_{SNRSTH}	SNRST pulse HIGH time		500	–	–	ns
$t_{d(SNRST-DAT)}$	delay SNRST pulse to data		200	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HA and VA (horizontal and vertical sync input)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
AC characteristics parallel bus: P0, P2, ALE and $\overline{PSEN}$ (external ROM access); see Fig.8						
$t_{W(ALE)}$	ALE pulse width		–	62.5	–	ns
t_{AVLL}	address valid to ALE LOW		17	–	–	ns
t_{LLAX}	address hold after ALE LOW		20	–	–	ns
t_{LLIV}	ALE LOW to instruction input		–	–	96	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW		–	31.25	–	ns
$t_{W(PSEN)}$	$\overline{PSEN}$ pulse width		–	93.75	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction input		–	–	60	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$		0	–	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$		–	–	30	ns
t_{AVIV}	address to valid instruction input		–	–	128	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float		–	–	10	ns
DC characteristics microcontroller pins: P0, P1, $\overline{INT0}$, $\overline{INT1}$, T0, T1, RSTW, RSTR, SNDA, SNCL, ALE, $\overline{PSEN}$ and $\overline{EA}$						
V_{OH}	HIGH-level output voltage	I_{OH} = –0.06 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
I_{LI}	input leakage current		–	–	±10	μA
$C_{I/O}$	pin capacitance		–	–	10	pF
Analog Y, U and V input filters (3rd-order linear phase filter with notch at f_{CLK}); see Fig.6						
$f_{(-3dB)}$	3 dB down frequency		5.4	5.6	5.8	MHz
$\alpha_{(0.5)}$	attenuation at $\frac{1}{2}f_{CLK}$ (8 MHz)		7	8	–	dB
α_{sb}	stop band attenuation (after notch)		32	–	–	dB
f_{notch}	notch frequency	tuned to $\frac{1}{2}f_{CLK}$	15.3	16	16.7	MHz
$t_{d(g)}$	group delay	at 4 MHz signal frequency	52	55	58	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog Y, U and V output filters (3rd-order linear phase filter with notch at f_{CLK})						
$f_{(-3dB)}$	3 dB down frequency		11.3	11.7	12.1	MHz
$\alpha_{(0.5)}$	attenuation at $\frac{1}{2}f_{CLK}$ (16 MHz)		7	8	–	dB
α_{sb}	stop band attenuation (after notch)		32	–	–	dB
f_{notch}	notch frequency	tuned to $\frac{1}{2}f_{CLK}$	30.6	32	33.4	MHz
$t_{d(g)}$	group delay	at 8 MHz signal frequency	26	28	31	ns
$t_{d(g)(tol)}$	group delay tolerance between channels		–	–	5	ns

Notes

1. With AGC at −3 dB, Y full ADC range is obtained at V_i = 1.41 V; with AGC at 6 dB, Y full ADC range is obtained at V_i = 0.5 V; with AGC at −3 dB, U full ADC range is obtained at V_i = 1.89 V; with AGC at 6 dB, U full ADC range is obtained at V_i = 0.67 V; with AGC at −3 dB, V full ADC range is obtained at V_i = 1.48 V; with AGC at 6 dB, V full ADC range is obtained at V_i = 0.52 V; at AGC attenuation more than 0 dB, where the input signal has an amplitude above the nominal value, the input processing and transfer function may have decreased specification.
2. DNL is defined as deviation of the code length from the average code length in LSB;

   $$DNL = \max\left(\frac{q_n}{q_{av} - 1}\right)$$: 0.99LSB means no missing code.
3. Measurements taken using video analyzer VM700A at YUV output, control bit SEL_1FH (address 391H) set to logic 1, internal analog filters off, AGC gain (addresses 302H, 303H and 304H) set to 074H, digital processing in between, digital filters off, sampling frequency of 16 MHz.
4. Supply Voltage Ripple Rejection (SVRR) is a relative variation of the full scale analog input for a supply variation of 0.25 V over a frequency range from 20 Hz to 50 kHz. This includes $\frac{1}{2}f_V$, f_V, $2f_V$, f_H and $2f_H$ which are major load frequencies.
5. Measurements carried out using Modulation Domain Analyzer HP53310A after change of control bit PLL_OPEN (address 376H) from logic 1 to logic 0 (open to closed-circuit). Control bits PLL_CK (address 375H) set to logic 0. Control bits PLL_CD (address 375H) set to 7.
6. The outputs are able to drive an external low-pass filter without slewing. In f_H and $2f_H$ this filter is of the type as described in Fig.6. For calculating an output filter the typical output impedance is also given in Fig.6.
7. The output levels for U and V have 1 dB reserve headroom in case of a 75% saturated colour bar. The maximum levels are 1.33 V + 1 dB = 1.49 V for U and 1.05 V + 1 dB = 1.18 V for V. Due to 1 dB headroom the typical AGC setting to obtain 0 dB from input to output for U and V is 83.
8. The AC characteristics are in accordance with the I^2C-bus specification for fast mode (clock frequency maximum 400 kHz). Information about the I^2C-bus can be found in the brochure *"I^2C-bus and how to use it"* (order number 9398 393 40011).

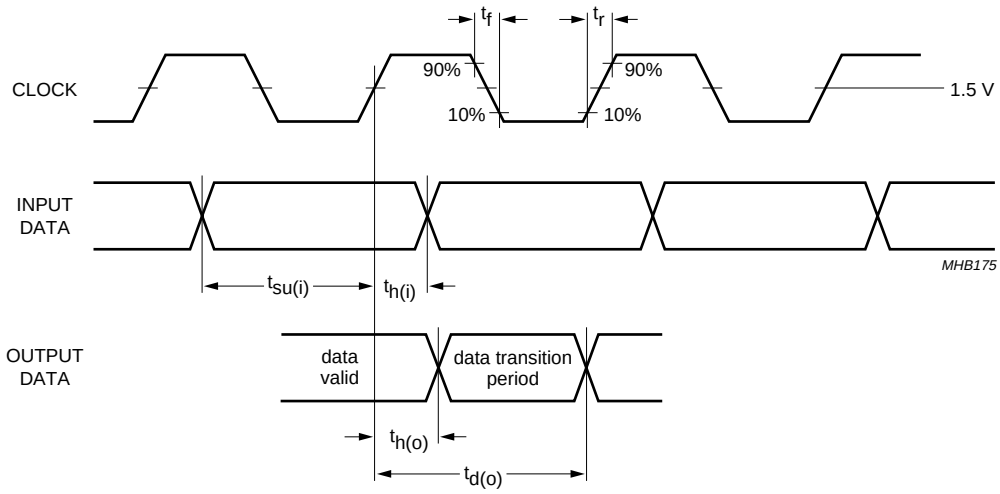


Fig.4 Data input/output timing diagram.

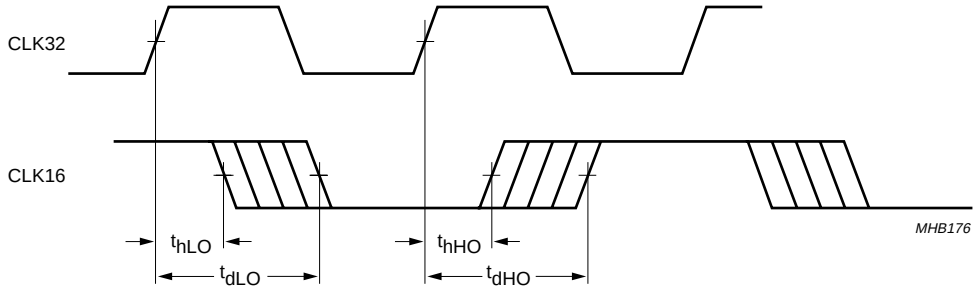
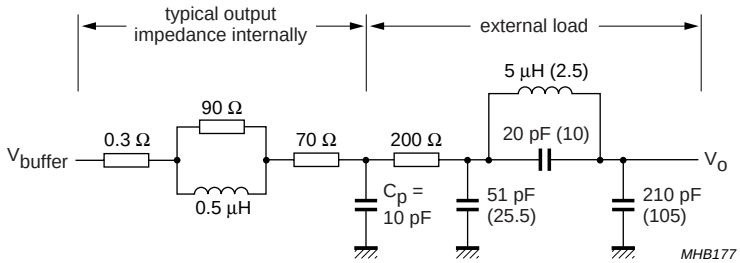


Fig.5 Timing relationship between CLK32 and CLK16.



Possible external load to be driven by output buffer without slewing.
C_p is including parasitic capacitance of the application.
Values in brackets are $2f_H$ mode.

Fig.6 Output load circuit.

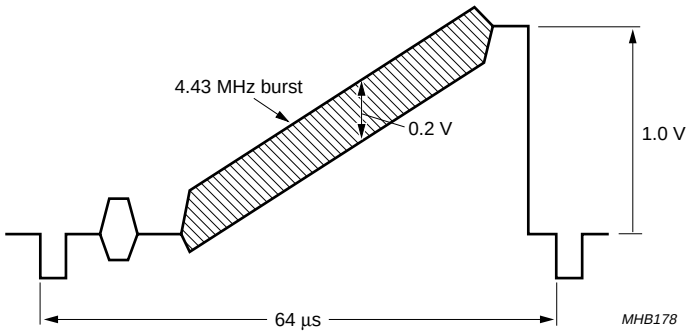


Fig.7 Test signal for differential gain and phase measurements.

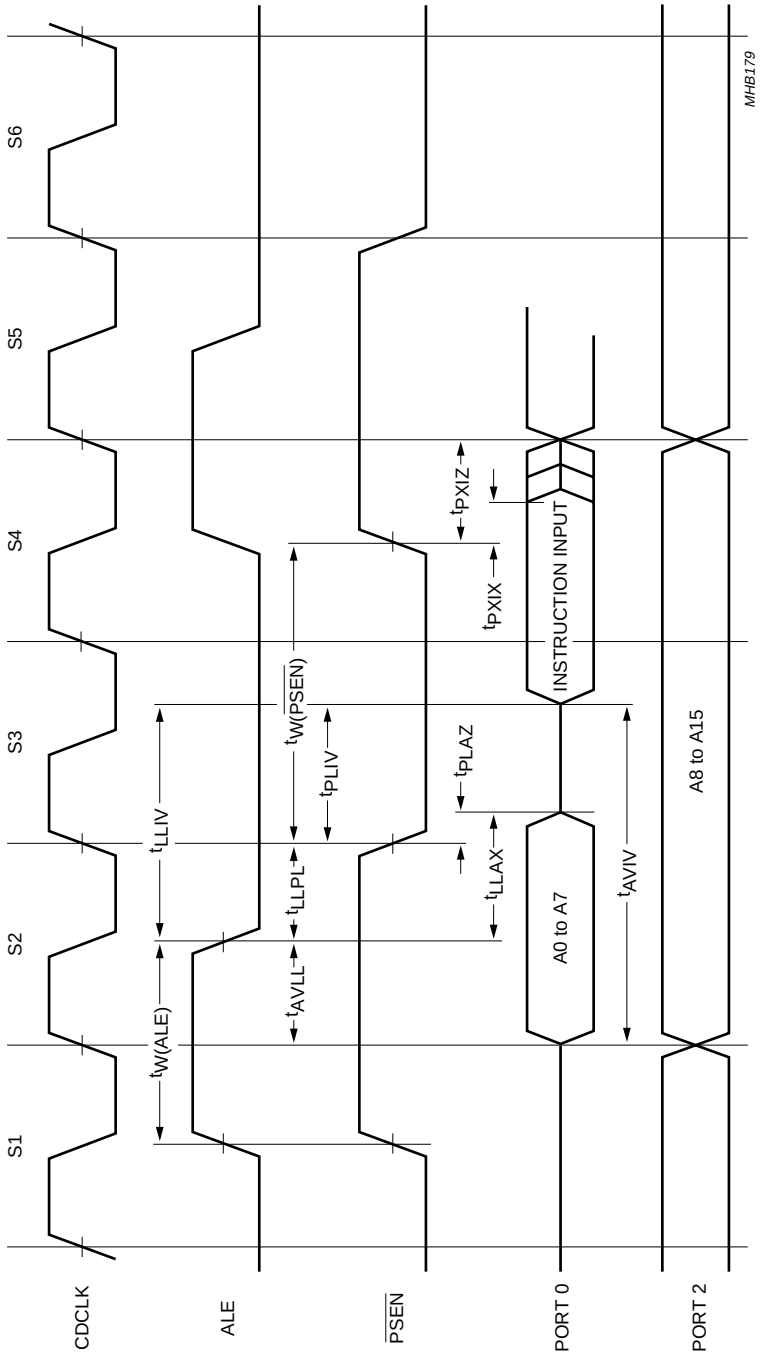


Fig.8 Program memory access timing.

Table 1 YUV formats; note 1

I/O PIN	4 : 1 : 1 FORMAT				4 : 2 : 2 FORMAT		4 : 2 : 2 FORMAT DOUBLE CLOCK				4 : 2 : 2 DPCM FORMAT	
YX8	Y07	Y17	Y27	Y37	Y07	Y17	U07	Y07	V07	Y17	Y07	Y17
YX7	Y06	Y16	Y26	Y36	Y06	Y16	U06	Y06	V06	Y16	Y06	Y16
YX6	Y05	Y15	Y25	Y35	Y05	Y15	U05	Y05	V05	Y15	Y05	Y15
YX5	Y04	Y14	Y24	Y34	Y04	Y14	U04	Y04	V04	Y14	Y04	Y14
YX4	Y03	Y13	Y23	Y33	Y03	Y13	U03	Y03	V03	Y13	Y03	Y13
YX3	Y02	Y12	Y22	Y32	Y02	Y12	U02	Y02	V02	Y12	Y02	Y12
YX2	Y01	Y11	Y21	Y31	Y01	Y11	U01	Y01	V01	Y11	Y01	Y11
YX1	Y00	Y10	Y20	Y30	Y00	Y10	U00	Y00	V00	Y10	Y00	Y10
YX0	Y0L	Y1L	Y2L	Y3L	Y0L	Y1L	U0L	Y0L	V0L	Y1L	Y0L	Y1L
UVX8	U07	U05	U03	U01	U07	V07	–	–	–	–	UC03	VC03
UVX7	U06	U04	U02	U00	U06	V06	–	–	–	–	UC02	VC02
UVX6	V07	V05	V03	V01	U05	V05	–	–	–	–	UC01	VC01
UVX5	V06	V04	V02	V00	U04	V04	–	–	–	–	UC00	VC00
UVX4	–	–	–	–	U03	V03	–	–	–	–	–	–
UVX3	–	–	–	–	U02	V02	–	–	–	–	–	–
UVX2	–	–	–	–	U01	V01	–	–	–	–	–	–
UVX1	–	–	–	–	U00	V00	–	–	–	–	–	–
UVX0	U0L	–	V0L	–	U03	V03	–	–	–	–	–	–

Note

1. Index X refers to different I/O buses:
   a) X = A: output to PALplus.
   b) X = B: input from PALplus, MPEG.
   c) X = C: output to first field memory for $2f_H$ applications.
   d) X = D: input from SAA4990H, SAA4991WP.

   The first index digit defines the sample number, the second defines the bit number.

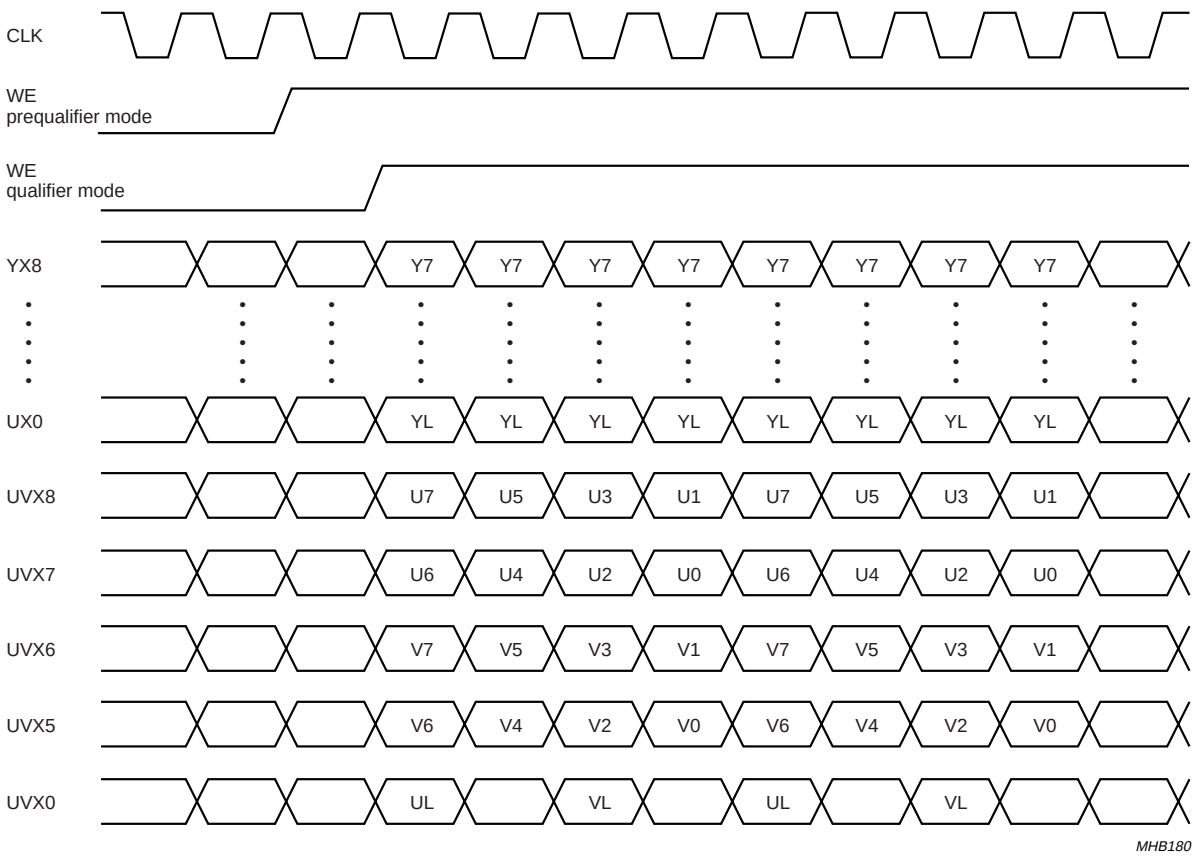


Fig.9 YUV data relationship defined by rising edge of WE in 4 : 1 : 1 format.

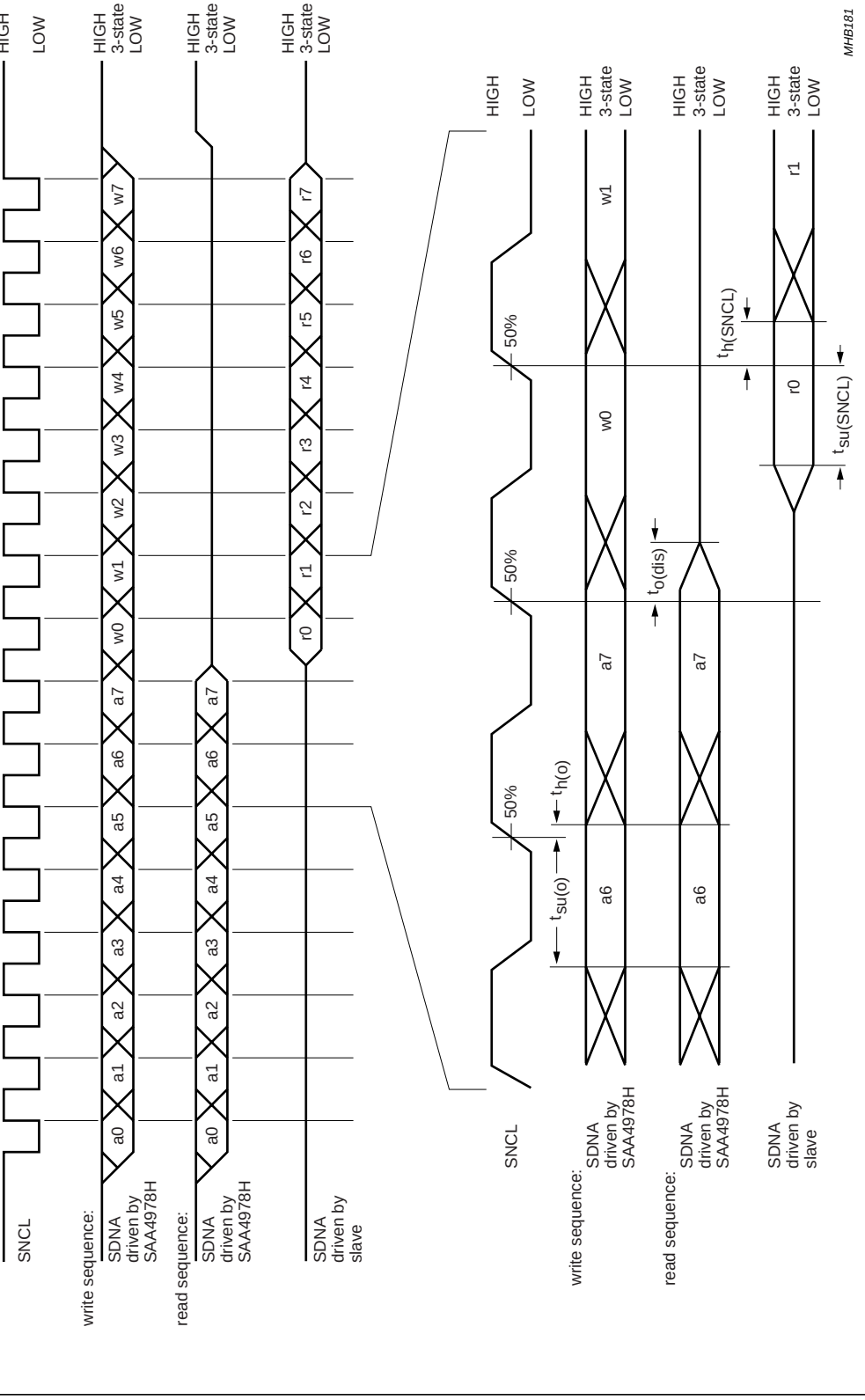


Fig.10 Timing diagram for SNERT bus.

12 APPLICATION INFORMATION

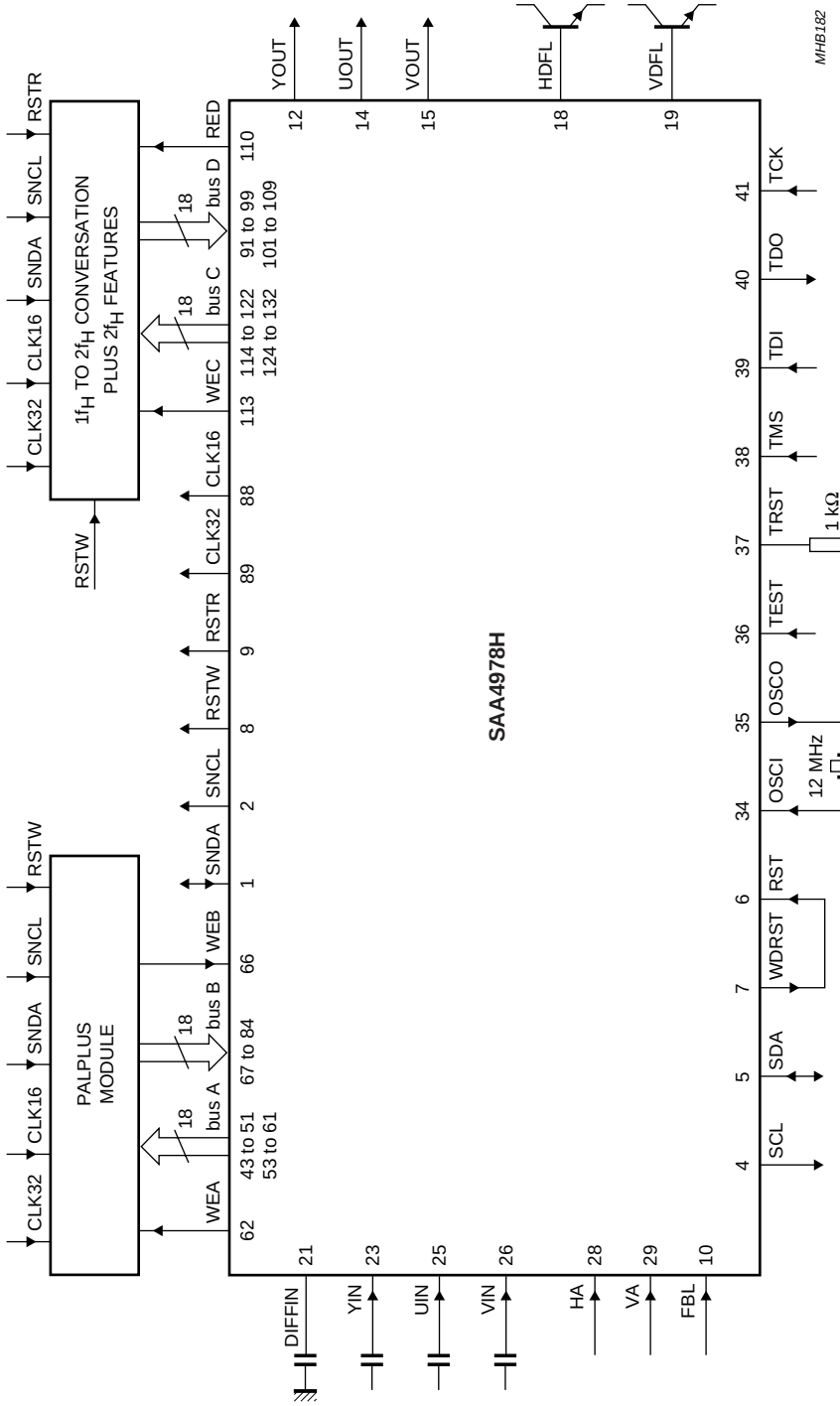


Fig.11 Application diagram.

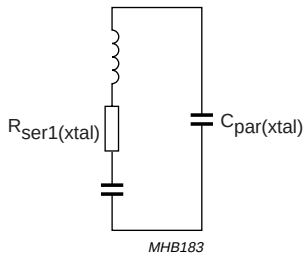


Fig.12 Equivalent circuit of crystal.

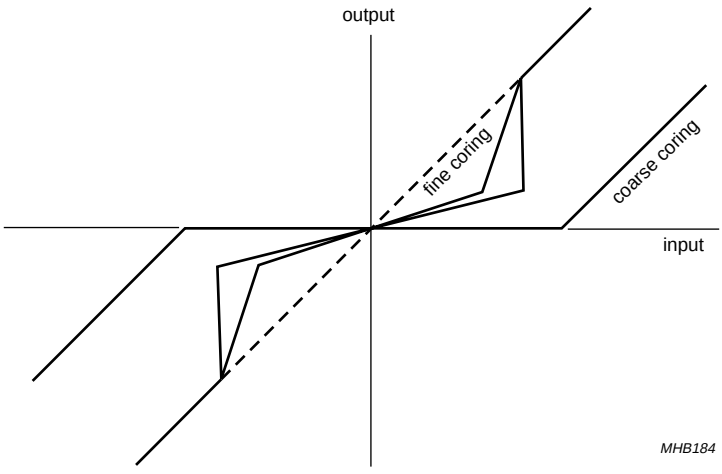
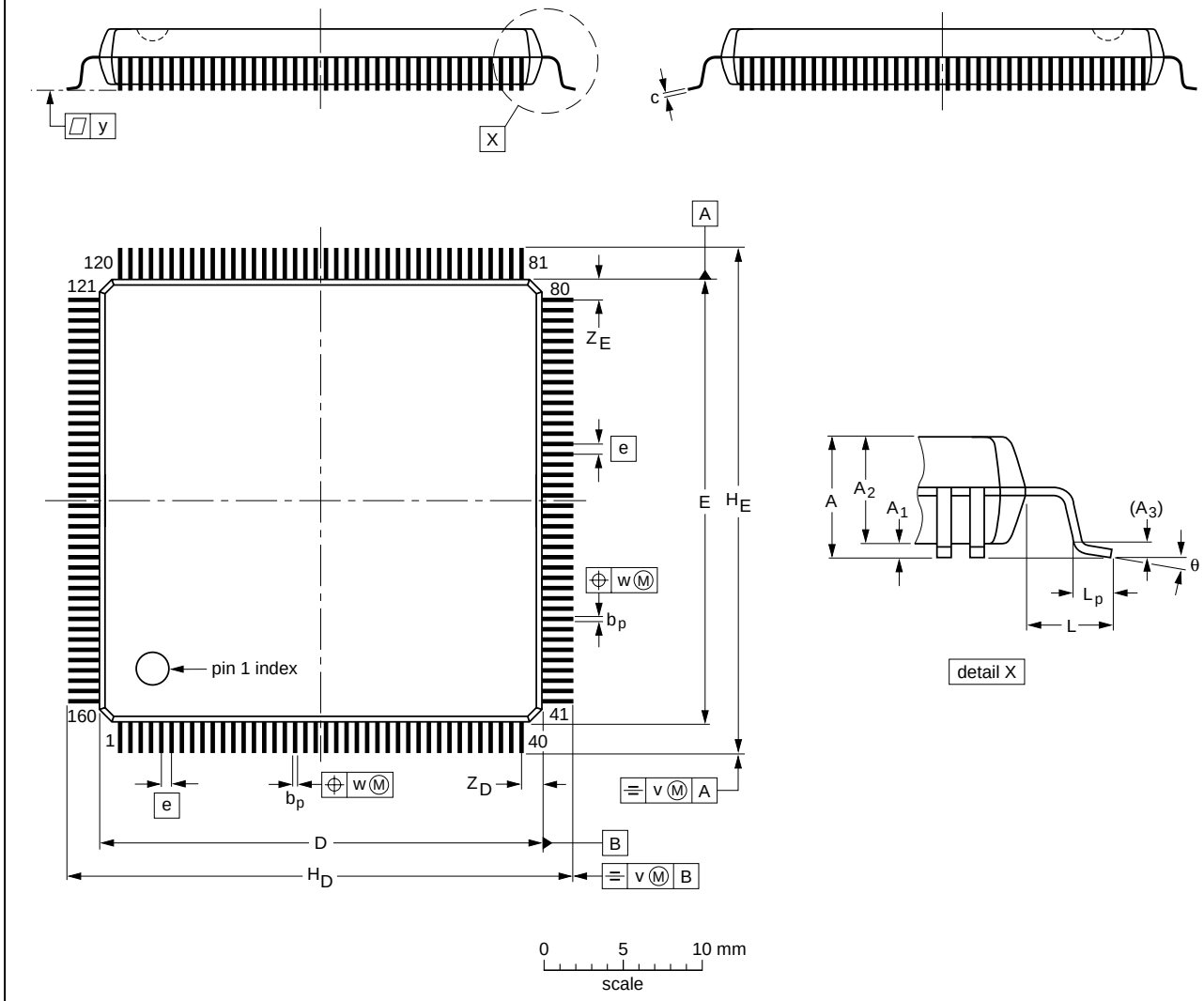


Fig.13 Peaking coring transfer curves.

13 PACKAGE OUTLINE

QFP160: plastic quad flat package;
160 leads (lead length 1.6 mm); body 28 x 28 x 3.4 mm; high stand-off height **SOT322-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	4.07	0.50 0.25	3.70 3.15	0.25	0.38 0.22	0.23 0.13	28.1 27.9	28.1 27.9	0.65	31.45 30.95	31.45 30.95	1.6	1.03 0.73	0.3	0.15	0.1	1.5 1.1	1.5 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT322-2		MO112DD1				~~96-03-14~~ 97-08-04

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

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